LSU EE 4720 **Homework 5** Solution **Due: 22 April 2016**

Problem 1: Solve Spring 2015 Final Exam Problem 3, which asks about the performance of several branch predictors. See older final exam solutions for more information on how to solve these kinds of problems.

See the final exam solution at `http://www.ece.lsu.edu/ee4720/2015/fe_sol.pdf`.

Problem 2: Show major elements of the hardware for each predictor used in Spring 2015 Final Exam Problem 3a. In particular:

- Show the BHT, PHT, and GHR (in those predictors that use them).
- Show the connection from the PC to the appropriate table.
- Show the number of bits in each connection.
- Show the logic generating a "predict taken" signal.

You **do not** need to show the logic to update the predictor or to generate the target address.

Solution appears below. The prediction is made using the MSB of the 2-bit counter, it it's 1 predict taken. Note that the size of the BHT here is ridiculously large, realistically the number of BHT entries would be on the order of 2^{14}.