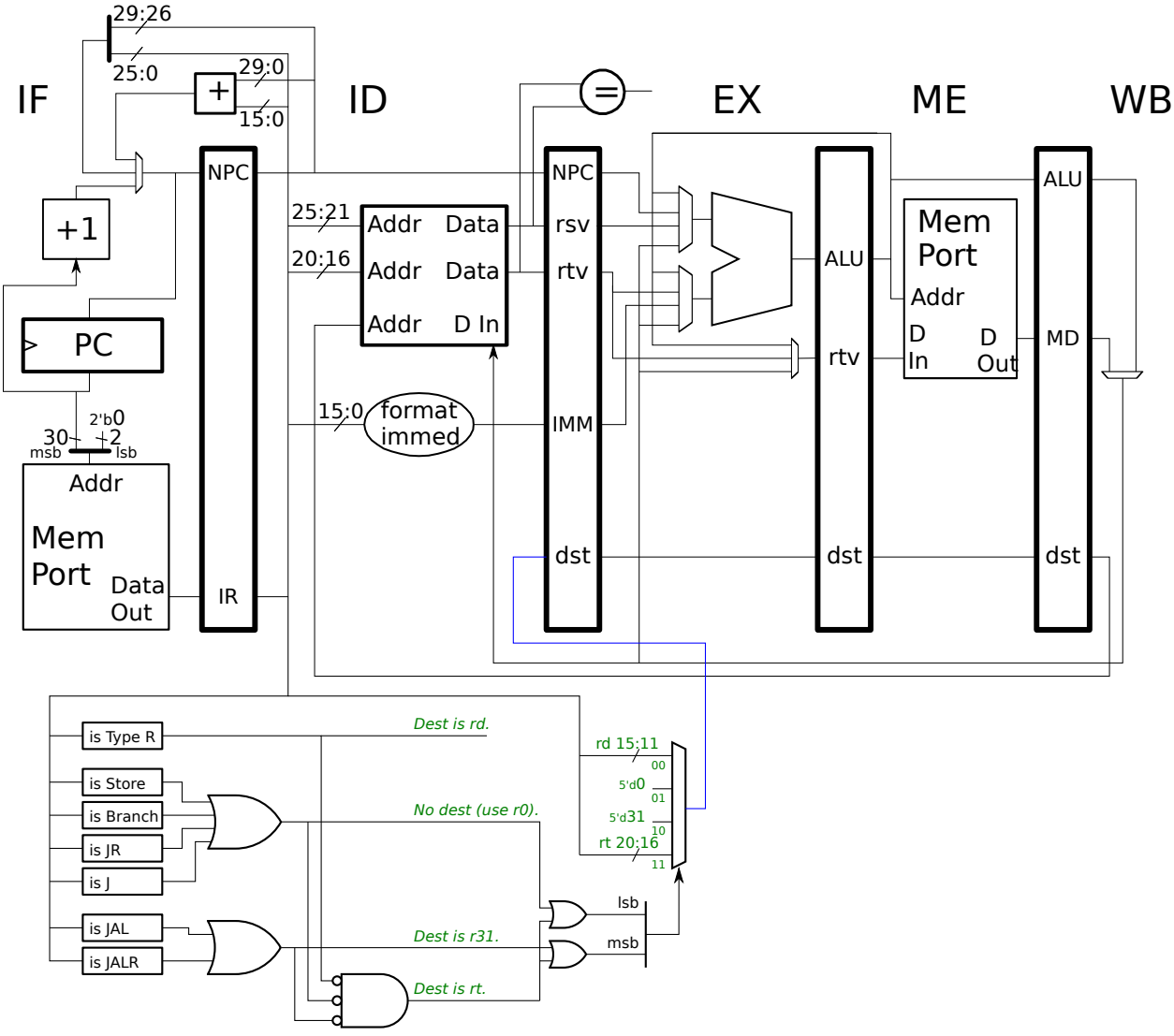
LSU EE 4720 **Homework 3** **Due: 28 March 2016**

Problem 1: Illustrated below is our MIPS implementation with some control logic shown. Modify the implementation so that it can execute the SPARC v8 instructions as described below. In your solution ignore register windows, assume that SPARC uses an ordinary 32-register general-purpose register file.

Details of the SPARC ISA (which includes later versions) can be found in `http://www.ece.lsu.edu/ee4720/doc/JPS1-R1.0.4-Common-pub.pdf`. An Inkscape SVG version of the illustration below can be found at `http://www.ece.lsu.edu/ee4720/2016/mpipei3b.svg`.



(*a*) Modify the implementation for format 3 arithmetic instructions. Use `add` as an example. Show changes in the bits used: to index the register file, to format the immediate, and to generate the writeback register number, `dst`.

(*b*) Modify the implementation for branch instructions. Use `BPcc` as an example. Be sure to make changes for computing the branch target.

Show changes in the hardware to generate the target address. Remove the unneeded MIPS branch comparison hardware and add a CC register.

(*c*) Modify the implementation for load and store instructions. Use `LDUW` and `STW` as examples.

Show changes in the format immediate unit, and make sure that it can handle both `ADD` and loads and stores.

Problem 2: Section 1.3.1 of the SPARC JPS1 lists features of the ISA.

(*a*) Indicate which features are typical RISC features and which features are not.

(*b*) One feature is "Branch elimination instructions" Provide an example of how such an instruction can be used to eliminate a branch.