Problem 1: Answer Spring 2014 Final Exam Problem 7(c), which asks about how new load addressing behavior should be added to MIPS.

Problem 2: Answer Spring 2014 Final Exam Problem 5, which asks about a new MIPS branch instruction, bfeq.

Problem 3: Show the control logic for the IF-stage multiplexor in the MIPS implementation below.

- The control logic should work for beq, bne, bgtz, bgez, and j. Assume that any other instruction is not a control transfer.
- Show exactly which IR bits are needed by the control logic that detects bgez (Hint, hint.) and other instructions.
- The control logic should check the condition to determine if the branch is taken.