EE 4755—Digital Design using Hardware Description Languages

Catalog Data

EE 4755 Digital Design Using Hardware Description Languages. (3) *Prereq: EE 3755 or equivalent.* Design of digital systems using a hardware description language (HDL). Structural and behavioral models as synthesis sources. Synthesis tools, coding for efficient synthesis. Coding strategies for common digital circuits.

Prerequisites by Topic

Logic design, computer organization, programming (C, C++, Java, etc.).

Textbook

To be announced.

Goals/Instructional Objectives

On entering the course students will have been exposed to an HDL (in prior courses) but will not be expected to know enough to carry through even a simple design to completion (synthesis). The course will cover in depth intermediate and advanced features of an HDL, and how those features are used to code designs of medium complexity. Such designs include a floating-point arithmetic unit, a CPU integer pipeline, or a GPU rasterization engine. The designs will be chosen based both on their complexity and on their relationship to other material in the curriculum. Students will also learn about synthesis and the relationship between their designs and the synthesized result. By the end of the course students should be able to complete a design of moderate complexity, making design trade-offs to balance cost and performance guided by data provided by synthesis tools, all of this using the same packages used by industry.

Homework Assignments and Projects

The assigned work will be a mix of short questions and problems (as in traditional homework) and of coding projects. The course outcomes can be met with a series of about four unrelated coding assignments or with a single term coding project in which students submit partially completed designs throughout the semester, culminating in a final submission.

For the coding projects students will use the same EDA tools used in industry. (The tools are routinely made available at low cost to academic institutions through some kind of higher education program, the ECE department has licensed tools through such programs at least since the year 2000.) As with a conventional laboratory course, students will receive hands-on experience with an engineering activity. The EDA tools are installed on ECE computers which students can access in workstation laboratories (with students using the machines any time during lab hours).

Course Learning Outcomes

At the end of the course the student will be able to:

- Use major features of a common HDL to develop HDL structural models, behavioral models, and testbenches.
- Code a design of moderate complexity in an organized manner, following well chosen style guidelines, resulting in a design that is easy to read, less likely to have flaws, and is easy to maintain.
- Run simulation tools to verify a design's functionality.
- Run synthesis tools to verify and tune timing and to prepare a design for fabrication.

Grading

Homework assignments, including HDL coding assignments, 30%; Midterm Exam, 35%; Final Exam, 35 %.

Topics

1 EDA Overview: Definitions of typical workflow and tools that are involved. *Classes: 3*, one at start of semester, other two much later.

2 Structural Descriptions: Representation of logic levels; primitives; expressions; modules. Basic synthesis tool usage. *Classes: 6*

3 Basic Synthesis Tool Usage: Design targets, timing and area constraints, design tuning. *Classes: 3*

4 Procedural Language Features: Variables and types, procedural constructs, event queue, etc. Testbench coding. *Classes: 9*

5 Behavioral Descriptions: Coding common building blocks. Inference of behavioral code by synthesis tools. *Classes: 9*

6 Design Examples: Coverage of design techniques and features through a medium-sized design. *Classes: 9*

7 Exams and Review: In-class midterm exam, review for midterm and final exams. *Classes: 3*