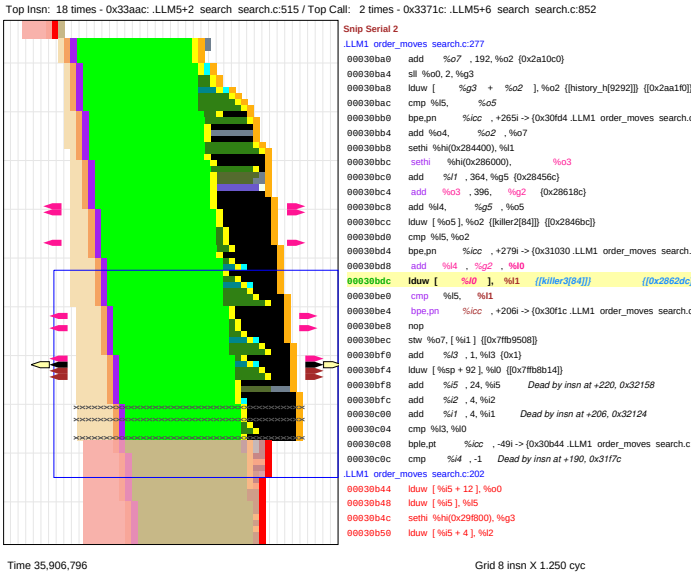
EE 4720: Computer Architecture

Syllabus

Where/When/Web/RSS

Room 1112 Patrick F. Taylor Hall
Monday Wednesday Friday 9:30–10:20 **Spring 2014**
`http://www.ece.lsu.edu/ee4720/`
`http://www.ece.lsu.edu/ee4720/rss_home.xml`



Who

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Tentative Office Hours: Monday–Friday: 14:00–15:00.

Topics

Instruction-Set Architecture and Microarchitecture
- Architecture and microarchitecture.
- Instruction set design and examples.

CPU Implementation
- Datapath components and basic pipelining techniques.
- Basic scheduling techniques.
- Get the most out of your datapath: dynamic scheduling (out-of-order execution).
- Branch and target prediction, and of course misprediction recovery.
- Provide more datapath: Superscalar, VLIW, and deeper pipelines.
- Parallel organizations: cluster, multi-core, many-core.

Memory System Implementation
- Caches.
- Virtual memory.

Text

Optional: "Computer architecture, a quantitative approach," John L. Hennessy & David A. Patterson, or "Computer organization & design," David A. Patterson & John L. Hennessy.

Grading

40% Midterm Exam • 40% Final Exam • 20% Homework
Final exam weight may be increased for students who show significant improvement on the final exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor's discretion either a makeup exam, use final exam grade for midterm grade (*i.e.*, 80% final exam weight), or use zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.