LSU EE 4720 Homework 7 Due: 1 November 2010

Problem 1: Do Spring 2010 Final Exam Problem 1 (our MIPS floating-point implementation questions). The following were the criteria used when grading the final. Positive numbers indicate total points for some aspect of the solution. Negative numbers are specific deductions for mistakes. Many of these are based on specific mistakes made by one or more students. In the criteria *smoke* means logic in which the outputs of two gates are connected together.

```
Problem 1 (15 pts)
^^^^^^^^^

 -2 Smoke

 4 Existing path for simple mtc1
   -2 Squiggly line starts in MEM.
   -2 Squiggly line from EX to fp RF din.

 4 Control Logic
   -3 Correct unbypassed mtc1, others wrong.
   -3 Compare sources to integer dest. Don't check insn types.
   -2 Bypass from FP add and M6 we, no test for reg# or int val. No mtc1.
   -4 and=>or of register field bit ranges, but inputs not connected.
   -1 Correct test for fd, but uses fs from ID, no test for type

 3 Store

 4 Bypasses
   -1 Store correct, other bypass could induce WF str hazard.
   -3 Bypass from output of ALU to A1 input.
   -2 Store bypass but no other bypass.
   -0 Correct mtc1 bypass, but no store bypass (and no store either).
   -4 Bypass from WF, with errors. (Mux out is 3rd input; src is fd).
   -3 Bypass from mem port data out to a1.
   -3 Bypass from EX/MEM.ALU, but connects to 1-input mux that smokes A1.
```

Problem 2: Do Spring 2010 Final Exam Problem 5 (how instructions given in problem could be added to MIPS). Grading criteria used in final exam (see previous problem):

```
Problem 5 (15 pts)
^^^^^^^^^

 5 Encoding
   -2 No attempt at field uniformity.
   -1 Show func as zero.
   -2 addsid: "immed=Mem[ ]"

 5 Shift Unit Placement
   -0 Mux rs and rsv; implicit assumption that ALU shifts.
   -2 Shift in ID or EX without mentioning critical path impact.
   -3 Assume that ALU can both shift and add.
   -2 slli: Use rsv for shift amount.
   -4 adds: Shift in ID, next cycle bypass from me. Omit stall, etc.
   -4 slli: Add a shift unit in ID stage. adds: shift before ALU, costly
   -5 sllii: "Only need shifter."  adds: "No hardware, use ALU for mult."
   -3 Direct connection ALU out to in. "much control logic"
   -0 "Control logic .. stalls .. ALU two consecutive cycles".

 5 Memory unit position
   -3 "Kind of" switching EX and ME.
   -3 Bypass from WB, that's hard. Omits stall, bypassing sources.
   -4 Bypass from WB, that's easy. Omits stall, bypassing sources.
   -4 No description of connections, but does note ME is after EX.
   -2 Memory port in ID, difficult. (Does not consider added stage.)
   -5 Difficult because of fetch, no datapath description.
   -0 "No extra dp.. reuse .. break pipe flow .. sig drops perf"
```