LSU EE 4720 **Homework 1** **Due: 3 March 2010**

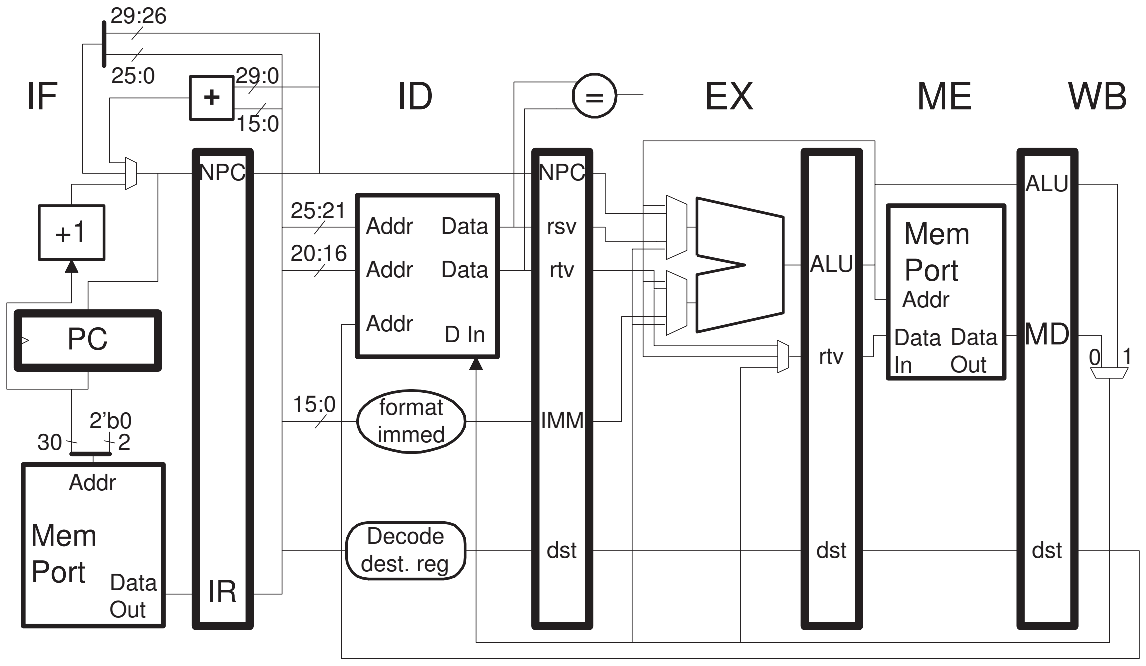
Problem 1: Re-write each code fragment below so that it uses fewer instructions (but still does the same thing).

```
# Fragment 1
lw r1, 0(r2)
addi r2, r2, 4
lw r3, 0(r2)
addi r2, r2, 4

# Fragment 2
slt r1, r2, r3
blt r1, r0  TARG
add r4, r5, r6

# Fragment 3
ori r1, r0, 0x1234
sll r1, r1, 16
ori r1, r1, 0x5678
```

Problem 2: The MIPS code below runs on the illustrated implementation. Assume that the number of iterations is very large.



```
LOOP:
 lw r3, 0(r1)
 addi r2, r2, 1
 beq r3, r4 LOOP
 lw r1, 4(r1)
```

(*a*) Show a pipeline execution diagram with enough iterations to determine the CPI.

(*b*) Determine the CPI.

(*c*) Schedule (re-arrange) the code to remove as many stalls as possible.

Problem 3: The MIPS implementation below has three multiplexors in the EX stage.

(*a*) Write a program that executes without stalls and which uses the eight ALU multiplexer inputs in order (perhaps starting at cycle 3) in consecutive cycles. That is, in cycle 3 the top input of the upper ALU mux would be used, (bypass from memory), in cycle 4 the second one would be used (NPC), in cycle 5 rsv, in cycle 6 bypass from WB, in cycle 7 we switch to the lower ALU mux with the bypass from ME input, in cycle 8 rtv, etc.

(*b*) Explain why it would be impossible to use the EX-stage rtv mux inputs in order in consecutive cycles.