EE 4720: Computer Architecture

Syllabus

Where/When/How/URL
Room 1110 CEBA Building
Monday Wednesday Friday 12:40–13:30 Fall 2006
Call Number 1925
http://www.ece.lsu.edu/ee4720/
RSS: http://www.ece.lsu.edu/ee4720/rss_home.xml

Who
David M. Koppelman
Room 349 Electrical Engineering Building
578-5482, koppel@ece.lsu.edu, http://www.ece.lsu.edu/koppel
Office Hours: Monday–Friday: 9:00–10:00.

Topics
Instruction-Set Architecture and Microarchitecture
   Architecture and microarchitecture (implementation).
   Instruction set design and examples.

CPU Implementation
   Datapath components.
   Basic pipelining techniques.
   Basic scheduling techniques.
   Dynamic scheduling, register renaming techniques.
   Branch and target prediction, speculation, and, of course, misprediction recovery.
   Multiple instruction issue: superscalar and VLIW/EPIC.

Memory System Implementation
   Locality, the computer engineer’s best friend.
   Caches.
   Virtual memory.

Text
“Computer architecture, a quantitative approach,” John L. Hennessy & David A. Patterson, or

Grading
40% Midterm Exam • 40% Final Exam • 20% Homework
Final exam weight may be increased for students who show significant improvement on the final exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor’s discretion either a makeup exam, use final exam grade for midterm grade (i.e., 80% final exam weight), or use zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.