

When / Where

Friday, 1 April 2005, 11:40-12:30 CST

CEBA 1114 (Here)

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm \times 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Solved tests and homework:. <http://www.ece.lsu.edu/ee4720/prev.html>

Statically Scheduled MIPS Study Guide:...

... <http://www.ece.lsu.edu/ee4720/guides/ssched.pdf>

Study Recommendations

Study this semester's homework assignments. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Previous Midterms

Implementation Diagrams and Pipeline Execution Diagrams

They are a *team*, so study them together.

Instruction Use

Should be able to easily understand MIPS programs.

Should be able to use other instructions in examples.

For example, SPARC, DLX, etc.

Not required to memorize instruction names, except for common MIPS instructions.

Introductory Material

ISA v. Implementation.

CPU Performance Equation

Benchmark types.

Compiling and Optimization

SPEC Benchmark Suite

SPEC membership and their interests.

Benchmark programs (types, how they were selected).

Rules for running benchmarks and disclosing results.

Compilers and Optimization

Basic optimization techniques, compiler optimization switches.

Profiling.

Compiler ISA and implementation switches.

How programmer typically uses compiler switches (options).

Instruction Set Design

Data Types: What to include, what to leave out.

Basic integer and floating point

Packed types: BCD, integer, saturating integer.

Size choices.

Memory and Register Organization

Stack and accumulator architectures.

Memory/Memory, Register/Memory.

Addressing Modes: What they do, which ones to include.

Register, Immediate, Direct, Register Deferred (Register Indirect), Displacement, Indexed, Memory Indirect, Autoincrement, Autodecrement, Scaled.

Control Transfer Instructions: Types, when to use.

Branch, Jump, Jump & Link, Call, Return

Format of displacements in instruction.

Specification of condition: condition code registers, integer registers, loop counter.

Delayed and predicated instructions; prediction hints.

Instruction Coding.

Fixed-length, variable-length, and bundled instructions.

Splitting of opcode field (as in MIPS type-R instructions).

ISA Classifications: RISC, CISC, VLIW, Stack, Accumulator

Synthetic Instructions

MIPS and DLX

Classification: RISC

Goals: ISA should allow simple, high-speed implementation.

Instruction types.

Know how to read and write MIPS programs.

Statically Scheduled MIPS Implementations

Unpipelined Implementation

Pipelined Implementations

Basic (2-cycle branch penalty).

Zero-cycle branch penalty.

Bypassed.

Dependency Definitions

Hazard Definitions

For a Given Pipelined Implementation

Show pipeline execution diagrams.

Show register contents at any cycle.

Determine control hardware.

Determine CPI.

Interrupts and Exceptions and Traps

Difference between interrupt, exception, trap.

Causes of exceptions, role of handler.

Privileged Mode.

Pipeline activity leading to execution of handler.

SPARC trap mechanism. (Trap base register, etc.).

Precise exceptions, achieving with floating-point operations.

Long Latency Operations

Types of operations. (Floating point and maybe load.)

Degree of pipelining: Initiation interval, latency.

Detecting functional unit structural hazards.

Detecting WB structural hazards: reservation register.

Detecting and handling RAW hazards: ID-stage v. pre-WB stall.

Loop Unrolling