LSU EE 4720 Homework 1 Due: 15 September 2004

Problem 1: Select two pairs of disclosures (that's four total) from the CPU2000 benchmark results posted at `www.spec.org`. A pair should be for machines using the same ISA but having different implementations. Make the implementations as different as possible. Explain why you think the implementations are very different.

Some ISAs and implementations are listed in lecture set 1, but the solution is not restricted to those. Feel free to ask if you're not sure what ISA a processor implements or whether two ISAs are considered the same or different.

For each disclosure list: the ISA, the implementation, the peak (result) performance, and file name of the HTML-formatted disclosure.

Problem 2: The processors below have roughly the same SPEC CINT2000 peak (result) scores but are very different. (The links should be clickable in Acrobat Reader.)

ISA: Power, Implementation: POWER5, Decode: 5-way Superscalar*
Disclosure: `http://www.spec.org/osg/cpu2000/results/res2004q3/cpu2000-20040804-03314.pdf`

ISA: Itanium (IA-64), Implementation: Itanium 2, Decode: 6-way Superscalar*
Disclosure: `http://www.spec.org/osg/cpu2000/results/res2004q1/cpu2000-20040126-02775.pdf`

ISA: IA-32, Implementation: Xeon, Decode: 3-way Superscalar*
Disclosure: `http://www.spec.org/osg/cpu2000/results/res2004q3/cpu2000-20040727-03291.pdf`

ISA: ≈IA-32, Implementation: Athlon, Decode: 3-way Superscalar*
Disclosure: `http://www.spec.org/osg/cpu2000/results/res2003q3/cpu2000-20030908-02502.pdf`

ISA: SPARC V9, Implementation: SPARC64 V, Decode: 4-way Superscalar*
Disclosure: `http://www.spec.org/osg/cpu2000/results/res2004q2/cpu2000-20040518-03044.pdf`

(*a*) The performance of the processors, based on the peak result, are roughly the same. On the same graph plot the performance in the following ways:

- Using the SPEC peak (result) scores.
- Assume that performance is proportional to clock frequency. Determine the score of a processor by comparing its clock frequency to that of the SPARC64 and using that to scale the SPARC64 peak result.
- The table above shows how many instructions a processor can decode per cycle. (Four-way superscalar means four per cycle, see explanation below.) Determine the performance by comparing the number of instructions fetched per second to the SPARC64 and use that to scale the SPARC64 peak result.

What conclusions can be drawn from the plotted data?

**The following information is not needed to solve this assignment. The decode widths shown above are the maximum number of instructions that can be decoded per cycle. For any real program the number will be much lower due to a variety of factors, which will be covered later in the semester. One relatively minor factor is the instruction mix. The POWER5 (implementation), Itanium (ISA), and to a lesser extent the others limit the kinds of instructions that can be decoded together. More on this later in the semester. The decode widths for the Xeon and Athlon don't refer to IA-32 instructions: these processors take IA-32 instructions and break them into simpler instructions called micro-ops by Intel and (favoring marketing over descriptive accuracy) macro-ops by AMD. The three instructions per cycle for the Xeon and Athlon are actually three micro- or macro-ops per cycle.*

(*b*) The Xeon and Athlon systems in the disclosures above have about the same performance. AMD might argue that those disclosures don't show the full potential of the Athlon. Find a system that uses an Athlon and scores much better, and explain what accounts for the difference.

(*c*) There is a system characteristic that affects the performance of benchmark mcf. What is it?

(*d*) Nominate a disclosure for The Most Desperate Peak Tuning award.