Fall 2013 Midterm Exam Review

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When / Where

Wednesday, 30 October 2013, 8:30-9:20 CDT

1110 Patrick F. Taylor Hall (Here)

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Lecture "slides" used in class: `http://www.ece.lsu.edu/ee3755/ln.html`

Study Guides

CLA: `http://www.ece.lsu.edu/ee3755/2013f/cla.pdf`

Synthesis: `http://www.ece.lsu.edu/ee3755/guides/syn.pdf`

Solved tests and homework:. `http://www.ece.lsu.edu/ee3755/prev.html`

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Topics for Exam

Everything up to and including Set 9, MIPS basic (pseudo instructions).

Material in lecture slides and homework.

Study Recommendations

Study this semester's homework assignments. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Previous Midterms

Be sure to look at previous midterms.

Emphases, Key Skills

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Verilog—Key Skills

Given a design in one form, write design in another:

- Explicit Structural
- Implicit Structural
- Synthesizable Behavioral
- Logic Diagram

Study Suggestion

Brown & Vranesic, Appendix A, elsewhere in text.

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Logic Design Skills

Given a design, be able to:

Compute Cost

Compute Delay

Study Suggestion

CLA Handout,

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Topics

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Verilog, The Simulation Language

Value Set

Know what `x` and `z` mean and how to generate and use them.

Modules and Instantiation

Continuous Assignment and Expressions

Implicit v. Explicit Structural Descriptions

Behavioral Code

Study Suggestion

Brown & Vranesic, Appendix A, elsewhere in text.

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Verilog, Design Flow and Synthesis

HDL Terminology

Brown & Vranesic, Section 2.9

Design Flow

Inference and Libraries

Combinational Logic Synthesis

Sequential Logic Synthesis

Study Suggestion

Synthesis Handout,

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Computer Arithmetic

Integer Adders

Carry Lookahead

Brown & Vranesic, Section 5.4

Hierarchical Adders

CLA Handout,

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Integer Multipliers

Patterson & Hennessy, 4th Ed., Section 3.3

Simple and streamlined multipliers.

Ordinary radix-n multiplier and Booth recoding multiplier.

Integer Dividers

Patterson & Hennessy, 4th Ed., Section 3.4

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FP Arithmetic

Patterson & Hennessy, 4th Ed., Section 3.5

Working with numbers in binary scientific notation.

IEEE 754 Format

FP Adder

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MIPS

Definitions

Patterson & Hennessy, 4th Ed., Sections 2.1, 2.2, 2.12

Integer Arithmetic and Logical Instructions

Patterson & Hennessy, 4th Ed., In chapter 2

Instruction Coding

Patterson & Hennessy, 4th Ed., Section 2.5

Pseudo Instructions

Patterson & Hennessy, 4th Ed., Section 2.12