LSU EE 3755 Homework 2 Solution Due: 25 September 2013

Read the carry lookahead handout before solving this assignment. It is linked to the course lecture notes page, `http://www.ece.lsu.edu/ee3755/ln.html`.

Problem 1: The handout mentions two types of CGL, *lookahead* and *ripple* but only describes lookahead CGL. The ripple CGL would generate c_i in terms of c_{i-1} as well as p_{i-1} and g_{i-1}. Show the logic for that as a Verilog module. The module should have three 1-bit inputs, and a 1-bit output.

Hint: To solve this problem draw a truth table with a_{i-1}, b_{i-1}, and c_{i-1} as inputs and g_{i-1}, p_{i-1}, and c_i as outputs. Of course, you can easily fill in the g and p values. From this table you should be able to figure out a function for c_i in terms of just c_{i-1}, p_{i-1}, and g_{i-1}. WARNING: figure this out for yourself, don't look for a solution elsewhere.

Solution appears below.

```
module cgl_ripple(co, ci, p, g);
   input ci, p, g;
   output co;

   assign co = ci && p || g;

endmodule
```

Problem 2: At the time this homework was assigned the CLA handout did not (yet) provide a delay analysis for the hierarchical CLAs. Provide a delay analysis for each of the variations given below. Use the *unrealistic* and *conservative* models from the slides.

To solve this problem one must understand two things. First, how a hierarchical CLA is constructed. Second, how to do the timing analysis.

Consider the "hierarchical CLA with lookahead CGL and a CLB-r" referred to part (b). This is constructed by using an l-bit ripple adder in the CLB and using lookahead CGL to compute the c_1 through c_m in terms of the carry in and P_0 to P_{m-1}, G_0 to G_{m-1}. See the illustration in the solution to part (b).

For the timing analyses needed for the sub-problems below use the following method: Start by marking all inputs with a zero (indicating $t = 0$). Look for a gate in which each input is marked. Take the maximum-valued mark and add on the gate delay. Mark the output of the gate with the sum. Repeat until all wires are marked. The delay is the highest value marked on an output.

In the unrealistic model XOR gates have a delay of 2, and all other gates have a delay of 1. In the conservative model a 3-input XORs gate has a delay of 1, all other gates have a delay of $\lg n$, where n is the number of inputs.

One can save time by identifying the *critical path* and only marking it. For the problems below the critical path has four parts: It starts with the G_0 signal. (P_0 is not critical because it uses one less layer of gates.) It then continues into the m-input CGL and out through output c_{m-1} into block CLB-x. In CLB-x the path goes into the l-bit adder. For CLB-r blocks the l-bit adder is a ripple adder and the third part of the critical path goes through $m-1$ bits of carry logic. For CLB-c blocks the third part goes through another CGL block. The last part of the critical path is through the XOR gate in bit $m-1$ of the adder.

See the solution to part (b) for a diagram showing delays along the critical path.

A common mistake was to compute the delay through a CLB in isolation, then compute the delay through the CGL in isolation and then add the two. That's a mistake in this case because the a and b inputs to CLB arrive before the c input. For the unrealistic model of a CLB-c, the delay is 5 from the a inputs but only 4 from the c input.

Detailed timing for each case is shown below.

(*a*) Provide a delay analysis for a hierarchical CLA with lookahead CGL and a CLB-c (blocks use CLAs). Show both unrealistic and conservative delays.

Unrealistic:

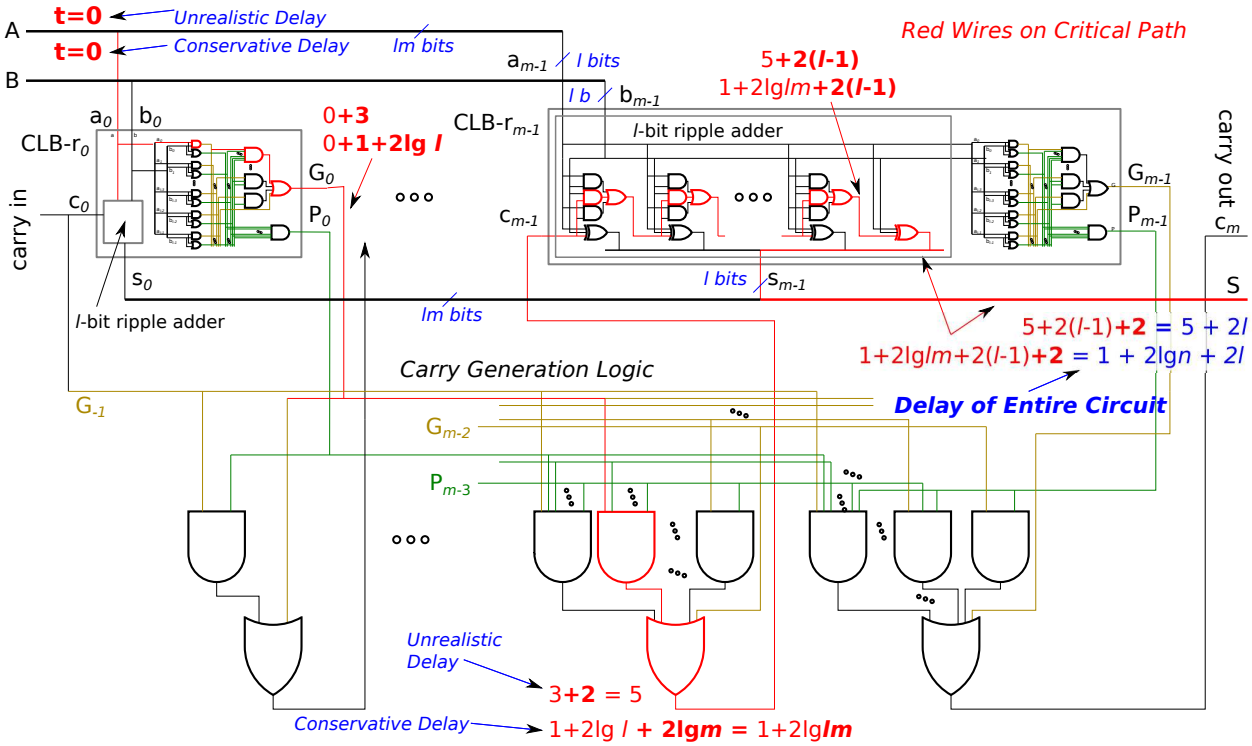
This Step	*Total*	*Signal produced in this step.*
0	0	Inputs (A, B, carry in)
2	2	P_i generated within CLB-c.
3	3	G_i generated within CLB-c.
2	5	c_i generated by the m-input lookahead CLG outside the CLB-c's.
2	7	c_i generated by the l-input lookahead CLG inside the CLB-c's.
2	9	The s_i generated by a CLC inside the adder in the CLB-c's.

Conservative:

This Step	*Total*	*Signal produced in this step.*
0	0	Inputs (A, B, carry in)
$1 + \lg l$	$1 + \lg l$	P_i generated within CLB-c.
$1 + 2 \lg l$	$1 + 2 \lg l$	G_i generated within CLB-c.
$2 \lg m$	$1 + 2 \lg l + 2 \lg m$	c_i generated by the m-input lookahead CLG outside the CLB-c's.
$2 \lg l$	$1 + 4 \lg l + 2 \lg m$	c_i generated by the l-input lookahead CLG inside the CLB-c's.
2	$3 + 4 \lg l + 2 \lg m$	The s_i generated by a CLC inside the adder in the CLB-c's.

(*b*) Provide a delay analysis for a hierarchical CLA with lookahead CGL and a CLB-r (blocks use ripple adders). Show both unrealistic and conservative delays.

The diagram below shows the critical path in red with both unrealistic and conservative delays shown long the path. After the diagram the delays are shown in tabular form.



Unrealistic:

This Step	*Total*	*Signal produced in this step.*
0	0	Inputs (A, B, carry in)
2	2	P_i generated within CLB-c.
3	3	G_i generated within CLB-c.
2	5	c_i generated by the m-input lookahead CLG outside the CLB-c's.
$2(l-1)$	$5+2(l-1)$	The c_{l-1} for the ripple adder inside a CLB-r.
2	$7+2(l-1)$	The s_{l-1} for the ripple adder inside a CLB-r.

Conservative:

This Step	*Total*	*Signal produced in this step.*
0	0	Inputs (A, B, carry in)
$1+\lg l$	$1+\lg l$	P_i generated within CLB-c.
$1+2\lg l$	$1+2\lg l$	G_i generated within CLB-c.
$2\lg m$	$1+2\lg lm$	c_i in the m-input lookahead CLG outside the CLB-c. (Note $\lg a+\lg b=\lg ab$).
$2(l-1)$	$-1+2\lg lm+2l$	c_{l-1} generated by the l-input lookahead CLG inside the CLB-c's.
2	$1+2\lg lm+2l$	The s_{l-} generated by a CLC inside the adder in the CLB-c's.

(c) Provide a delay analysis for a hierarchical CLA with ripple CGL and a CLB-r (blocks use ripple adders). Show both unrealistic and conservative delays.

Unrealistic:

This Step	*Total*	*Signal produced in this step.*
0	0	Inputs (A, B, carry in)
2	2	P_i generated within CLB-c.
3	3	G_i generated within CLB-c.
$2(m-1)$	$1+2m$	c_{m-1} generated by the m-input lookahead CLG outside the CLB-c's.
$2(l-1)$	$-1+2m+2l$	The c_{l-1} for the ripple adder inside a CLB-r.
2	$1+2m+2l$	The s_{l-1} for the ripple adder inside a CLB-r.

Conservative:

This Step	*Total*	*Signal produced in this step.*
0	0	Inputs (A, B, carry in)
$1+\lg l$	$1+\lg l$	P_i generated within CLB-c.
$1+2\lg l$	$1+2\lg l$	G_i generated within CLB-c.
$2(m-1)$	$-1+2\lg l+2m$	c_{l-1} of the m-input ripple CLG outside the CLB-c's.
$2(l-1)$	$-2+2\lg l+2(m+l)$	c_{l-1} generated by the l-input lookahead CLG inside the CLB-c's.
2	$2\lg l+2(m+l)$	The s_{l-} generated by a CLC inside the adder in the CLB-c's.