LSU EE 3755 Homework 2 Due: 25 September 2013

Read the carry lookahead handout before solving this assignment. It is linked to the course lecture notes page, `http://www.ece.lsu.edu/ee3755/ln.html`.

Problem 1: The handout mentions two types of CGL, *lookahead* and *ripple* but only describes lookahead CGL. The ripple CGL would generate c_i in terms of c_{i-1} as well as p_{i-1} and g_{i-1}. Show the logic for that as a Verilog module. The module should have three 1-bit inputs, and a 1-bit output.

Hint: To solve this problem draw a truth table with a_{i-1}, b_{i-1}, and c_{i-1} as inputs and g_{i-1}, p_{i-1}, and c_i as outputs. Of course, you can easily fill in the g and p values. From this table you should be able to figure out a function for c_i in terms of just c_{i-1}, p_{i-1}, and g_{i-1}. WARNING: figure this out for yourself, don't look for a solution elsewhere.

Problem 2: The CLA handout does not (yet) provide a delay analysis for the hierarchical CLAs.

(*a*) Provide a delay analysis for a hierarchical CLA with lookahead CGL and a CLB-c (blocks use CLAs). Show both unrealistic and conservative delays.

(*b*) Provide a delay analysis for a hierarchical CLA with lookahead CGL and a CLB-r (blocks use ripple adders). Show both unrealistic and conservative delays.

(*c*) Provide a delay analysis for a hierarchical CLA with ripple CGL and a CLB-r (blocks use ripple adders). Show both unrealistic and conservative delays.