Fall 2012 Midterm Exam Review

mr-1

When / Where

Wednesday, 24 October 2012, 9:30-10:20 CDT

2142 Patrick F. Taylor Hall (Here)

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Lecture "slides" used in class: `http://www.ece.lsu.edu/ee3755/ln.html`

Solved tests and homework:. `http://www.ece.lsu.edu/ee3755/prev.html`

Topics for Exam

Everything up to and including branch instructions.

Material in lecture slides and homework.

Study Recommendations

Study this semester's homework assignments. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Previous Midterms

Be sure to look at previous midterms.

Emphases, Key Skills

mr-4

Verilog—Key Skills

Given a design in one form, write design in another:

Explicit Structural

Implicit Structural

Synthesizable Behavioral

Logic Diagram

Topics

mr-5

Verilog, The Simulation Language

Value Set

Know what `x` and `z` mean and how to generate and use them.

Modules and Instantiation

Continuous Assignment and Expressions

Implicit v. Explicit Structural Descriptions

Behavioral Code

mr-6

Verilog, Design Flow and Synthesis

HDL Terminology

Brown & Vranesic, Section 2.9

Design Flow

Inference and Libraries

Combinational Synthesis

Sequential Synthesis

mr-6

mr-7

Computer Arithmetic

Integer Adders

Carry Lookahead

Brown & Vranesic, Section 5.4

Two-Level Adders

mr-7

mr-8

Integer Multipliers

Patterson & Hennessy, 4th Ed., Section 3.3

Simple and streamlined multipliers.

Ordinary radix-n multiplier and Booth recoding multiplier.

Integer Dividers

Patterson & Hennessy, 4th Ed., Section 3.4

mr-9

FP Arithmetic

Patterson & Hennessy, 4th Ed., Section 3.5

Working with numbers in binary scientific notation.

IEEE 754 Format

FP Adder

mr-9

mr-10

MIPS

Definitions

Patterson & Hennessy, 4th Ed., Sections 2.1, 2.2, 2.12

Integer Arithmetic and Logical Instructions

Patterson & Hennessy, 4th Ed., In chapter 2

Control Transfer Instructions

Patterson & Hennessy, 4th Ed., In chapter 2

Instruction Coding

Patterson & Hennessy, 4th Ed., Section 2.5

Pseudo Instructions

Patterson & Hennessy, 4th Ed., Section 2.12