# LSU EE 3755 Homework 6 Due: 26 November 2012

*This assignment is to be completed on the ECE Linux workstations, please follow the instructions at* `http://www.ece.lsu.edu/ee3755/proc.html`.

**Problem 0:** Follow the instructions for MIPS Homework Workflow in the procedures page, `http://www.ece.lsu.edu/ee3755/proc.html`, but substitute `hw06` for the directory and `hw06.v` for the name of the file to copy. (The extension is `.v` (Verilog), not `.s` (assembler).)

Load the file into an Emacs buffer. If things are set up correctly the buffer should show most comments in red (though titles will be a larger black font) and Verilog code should by syntax-highlighted, for example showing `input` and `output` in light blue and `reg` in purple. There should also be a Verilog pull-down menu.

Run the Verilog simulation without modification by pressing `F9` or by selecting Verilog Compile. (Don't select synthesize and compile, it does not work yet.) The window should be split into two panes, with the lower pane starting with something like:

```
-*- mode: compilation; default-directory: "~/teach/co12f/s/" -*-
Compilation started at Mon Nov 19 08:05:19

irun -batch -exit hw06.v
irun(64): 10.20-s120: (c) Copyright 1995-2012 Cadence Design Systems, Inc.
file: hw06.v
module worklib.cpu:v
errors: 0, warnings: 0
```

and ending with something like

```
 PC 0x00400010:   10: li $a1, 10
 Register $5 (  a1): 0x00000032 (         50) -> 0x0000000a (         10)
 PC 0x00400014:   12: addi $t6, $0, -2
 Register $14 (  t6): 0x0000008c (        140) -> 0xfffffffe (         -2)
 PC 0x00400018:   13: addi $t5, $0, 2

 Register $13 (  t5): 0x00000082 (        130) -> 0x00000002 (          2)
 PC 0x0040001c:   15: bgez $t5, SKIP1
*** Illegal instruction exception at address 0x0040001c ***
Executed 8 instructions, average time 2.88 CPI.
End of testbench run.
```

The text "Illegal instruction exception" indicates that the simulated MIPS processor, in `hw06.v`, did not recognize an instruction. That will be fixed in Problem 2.

**Problem 1:** Change implementation of `lui` so that it uses the shift unit in the ALU rather than using a shifted version of the immediate, `limmed`. There is no way to tell if this is solved correctly just by looking at simulator output. But, if the modified implementation does not execute `lui` correctly there will be an error message. For example,

```
 PC 0x00400000:   6: lui $t1, 0x1234;
 Register $9 (  t1): 0x0000005a (         90) -> 0x00000000 (          0)
*** FAIL: Wrong value written.  0x12340000 (correct) != 0x00000000 ***
```

*Hint: Look at the way the* `sll` *instruction is implemented.*

**Problem 2:** The illegal instruction exception encountered above is due to the `bgez` instruction not being implemented by the MIPS module. Implement `bgez` and `bltz`, the simulation should run to completion (without showing an illegal instruction exception or other error messages) finishing with a "PASS" message.

For detailed descriptions of these instructions see `http://www.ece.lsu.edu/ee4720/mips32v2.pdf`.