EE 3755—Computer Organization

00-1

Call Number 1711 (Spring 2002)

URL: http://www.ece.lsu.edu/ee3755

Offered by:

David M. Koppelman

349 EE Building

578-5482, koppel@ece.lsu.edu, http://www.ece.lsu.edu/koppel/koppel.html

Tentative office hours: Mon 15:00-16:00; Wed 9:30-10:30; Tue & Thr 14:00-15:30.

Should already know...
... how to design with logic.

Will learn...
... how to design a rudimentary computer.

Prerequisites

00-2

Prerequisite by Course

EE 2730 (Digital Logic II) or equivalent.

Prerequisite by Topic

Logic design.

Binary number representation and arithmetic.

Programming of some kind.

Texts

00-3

"Computer organization & design," David A. Patterson & John L. Hennessy (Required).

"Verilog HDL," Samir Palnitkar (Optional).

Additional Verilog reference material on course Web page.

Graded Material

00-4

40% Midterm Exam

40% Final Exam

20% Homework (Roughly six assignments.)

Lowest homework grade dropped.

Short Course Outline

00-5

Hardware Description using Verilog

A commonly used language for designing digital hardware.

Computer Arithmetic

How computers add, subtract, multiply, and divide.

Integer and floating-point.

Will use Verilog to design circuits.

RISC Microprocessor Programming

The basics of programming an easy-to-program processor, MIPS.

Computer Organization

Design hardware to execute MIPS programs.

This material will be continued in EE 4720.

Detailed Course Outline

00-6

Digital Design Hardware Description Languages (HDLs)

Designs for digital parts captured in a *HDL description*.

Popular HDLs: Verilog, VHDL.

An HDL description is fed to:

A *simulator*, to see what the design does.

(Whether it does what it's supposed to do.)

A *synthesis program*, to prepare the design for fabrication or downloading.

Chips may be fabricated using the synthesized description.

The synthesized description might be downloaded to a special chip (FPGA).

00-7

HDL Material

Language used: Verilog

Subset of the language covered.

Enough to implement processor arithmetic units and other datapath elements.

00-7

00-8

HDL Topics Covered

Writing structural descriptions of hardware.

Writing simple behavioral descriptions of hardware.

Relationship between descriptions and synthesized hardware.

HDL Topics Not Covered

Less-common structural elements and delay specifiers.

Much event- and delay-related behavioral code.

Will not know enough to write a good *testbench*.

Thorough HDL treatment may be given in other courses.

00-9

HDL Software Used

Host System

ECE Sun systems.

Simulator

Model Technology (Mentor Graphics) ModelSim SE Plus

Synthesis

Exemplar (Mentor Graphics) Leonardo Spectrum

00-9

Computer Arithmetic Topics

00-10

Integer arithmetic algorithms. (Mostly review).

Integer adder implementations.

ALU implementation.

Basic integer multiplication and division implementations.

High-speed integer multiplier implementation.

Floating-point representations.

Floating-point arithmetic algorithms.

Floating-point adder implementation.

EE 3755 Lecture Transparency. Formatted 9:54, 23 January 2002 from lsli00.

00-10

RISC Microprocessor Topics

00-11

RISC Processor

A type of processor that became popular in 80's.

RISCs simple to program and to implement (design hardware for).

Simplicity allows high-speed implementation.

Starting in 80's all new major processors were RISCs ...
... until now with Intel's IA-64.

(IA-64 covered in EE 4720.)

00-11

00-12

RISC Families:

MIPS: Ownership: Independent, then Silicon Graphics, now ??.

PA (Precision Architecture): Ownership: Hewlett-Packard.

SPARC: Ownership: Sun Microsystems / SPARC International.

POWER, PowerPC: Ownership: IBM, Apple/IBM/Motorola.

Alpha: Ownership: DEC, Compaq.

MIPS used in Patterson & Hennessy text (and so used in class).

SPARC used in ECE computers.

00-13

Covered for the MIPS processor.

MIPS Processor organization:

What machine-language programs can access.

What machine-language instructions can do.

MIPS Programming

Subset of instructions covered.

Processors Covered in Other Courses

EE 3750 /3751: IA-32 (Intel 80x86, Pentium)

EE 4720: DLX, SPARC, some IA-64 and other architectures.

Computer Organization Topics

00-14

Building a "Toy" MIPS Processors

Use Verilog.

Topics

- Functional Simulator: Simple Design, Inefficient Hardware
- Multicycle Hardwired Control
- Multicycle Microprogrammed Control

Material continued in EE 4720.

EE 3755 Lecture Transparency. Formatted 9:54, 23 January 2002 from lsli00.

00-14