# EE 3755: Computer Organization

## *Syllabus*

## Where/When/How/URL

2150 CEBA Building
Monday Wednesday Friday 12:40–13:30 **Spring 2002**
Call Number 1711
`http://www.ece.lsu.edu/ee3755/`

## Who

David M. Koppelman
Room 349 Electrical Engineering Building
578-5482, `koppel@ece.lsu.edu`, `http://www.ece.lsu.edu/koppel/koppel.html`
Tentative Office hours: Mon 15:00-16:00; Tue & Thr 14:00-15:30 Wed 9:30-10:30.

## Topics

Introduction to Hardware Description Using Verilog

Computer Arithmetic
- Integer Add and Subtract Hardware
- Integer Multiplication Algorithms and Hardware
- Basic Integer Division Algorithm and Hardware
- IEEE 754 and Other Floating-Point Representations
- Floating-Point Addition Algorithm and Hardware
- Floating-Point Multiplication and Division Algorithms

Organization and Programming of a RISC Processor (MIPS)
- Registers, Memory, and Instruction Execution
- Assembly Language Programming

Basic Processor Implementation Techniques
- Datapath Elements (Registers, memory ports, etc.)
- Hardwired and Microprogrammed Control Techniques

## Text

"Computer organization & design," David A. Patterson & John L. Hennessy.
"Verilog HDL," Samir Palnitkar (Optional).

## Grading

40% Midterm Exam • 40% Final Exam • 20% Homework
Final exam weight may be increased for students who show significant improvement on the final exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor's discretion either a makeup exam, use final exam grade for midterm grade (*i.e.*, 80% final exam weight), or use zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.