Transistors

These are three terminal devices, where the current or voltage at one terminal, the input terminal, controls the flow of current between the two remaining terminals.
Transistors

Can be classified as:

- FET – Field Effect Transistor;
  - Majority carrier device;
  - Unipolar device;
- BJT – Bipolar Junction Transistor;
  - Minority carrier device;
  - Bipolar device.
FETs

Two primary types:

- MOSFET, Metal-Oxide-Semiconductor FET. Also known as IGFET – Insulated Gate FET;
- JFET, Junction FET.

MOS transistors can be:

- n-Channel;
  - Enhancement mode;
  - Depletion mode;
- p-Channel;
  - Enhancement mode;
  - Depletion mode;
MOSFET Structure
MOSFETs are identified by symbols like the ones shown below:
MOSFET Operation

- **Voltage at gate** controls the flow of current between drain and source.
- **$V_{GS}$** – Voltage between gate and source.
- **$V_{DS}$** – Voltage between drain and source.
MOSFET Operation

- When $V_{GS} = 0$ then no current flows between drain and source.
- pn-Junction is reverse biased.
Threshold Voltage

- The value of $V_{GS}$ where the drain current just begins to flow.
- Typical values:
  - 0.3 to 0.8 volts.
MOSFET Operation

Two cases:
- **Ohmic region:**
  \[ |V_{DS}| < |V_{GS} - V_T| \]
- **Active Region:**
  \[ |V_{DS}| > |V_{GS} - V_T| \]
MOSFET Operation

**Ohmic Region:**

\[ |V_{DS}| < |V_{GS} - V_T| \text{ and } |V_{GS}| > |V_T| \]

\[ I_D = K \left[ 2 \left( V_{GS} - V_T \right) V_{DS} - V_{DS}^2 \right] \]

\[ |V_{GS}| \ll |V_T| \]

\[ I_D = 0 \]
MOSFET Operation

**Active Region:**

\[
|V_{DS}| > |V_{GS} - V_T| \quad \text{and} \quad |V_{GS}| > |V_T|
\]

\[
I_D = K (V_{GS} - V_T)^2
\]

\[
|V_{GS}| \ll |V_T|
\]

\[
I_D = 0
\]
The constant \( K \), called the conductance parameter, is measured in units of mA/V\(^2\).

\[
K = \frac{1}{2} \mu_e C_{ox} \frac{W}{L}
\]

Where:

\[
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}
\]
MOSFET Output Curves

A family of curves representing the $V-I$ characteristics of transistors.

A plot of drain current, $I_D$, as a function of drain-to-source voltage, $V_{DS}$, for several values of $V_{GS}$.
Ohmic and Active Regions

\[ |V_{DS}| < |V_{GS} - V_T| \text{ and } |V_{GS}| > |V_T| \]

\[ I_D = K \left[ 2 \left( V_{GS} - V_T \right) V_{DS} - V_{DS}^2 \right] \]

\[ |V_{GS}| \ll |V_T| \]

\[ I_D = 0 \]

\[ |V_{DS}| > |V_{GS} - V_T| \text{ and } |V_{GS}| > |V_T| \]

\[ I_D = K \left( V_{GS} - V_T \right)^2 \]

\[ |V_{GS}| \ll |V_T| \]

\[ I_D = 0 \]
P-Channel Enhancement MOSFET

- Note the n-type body and the p-type source and drain areas.
- Both $V_{GS}$ and $V_{DD}$ are negative with respect to ground.
Depletion Mode MOSFETs

- n-Channel is built in.
- \( V_{GS} \) varies from negative values to positive values, where negative values of \( V_{GS} \) depletes the channel while positive values enhance it further.
JFETs

- Depletion-mode FET with a different structure than that of the MOSFET.
- Not generally used for switching elements of digital circuits.
- Used in special applications such as analog circuits where very high input impedance is required.
JFETs

Every $p$-$n$ junction has a depletion region devoid of carriers, and the width of the depletion region can be controlled by the applied voltage across the junction.
JFETs

- Note the highest value of $V_{GS}$.
- What happens if you make $V_{GS}$ positive with respect to ground.
Inverter Circuit

This circuit is designated as the *common source* configuration. It is used in digital circuits.
Inverter Circuit

- When $V_{in}$ is low the transistor is off and $V_{out}$ is high.
- When $V_{in}$ is high the transistor is on and $V_{out}$ is low.
MOSFET Circuit Model For Switching

$V_{GS}$ controls the switch in the model and $r_{on}$ is defined as:

$$r_{on} = \frac{1}{g_{on}} = \frac{1}{\left| \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{DS}=0}}$$

$$r_{on} = \frac{1}{K2(V_{GS} - V_T)}$$
Inverter Circuit

\[ V_{in} = 0 \]
\[ V_{out} = (+V_{DD}) \]
\[ V_{in} = V_{DD} \]
\[ V_{out} = \left[ \frac{r_{on}}{r_{on} + R_L} \right] (+V_{DD}) \]
\[ r_{on} \ll R_L, V_{out} \ll V_T \]
Inverter Circuit

For $R_L = 1\,K\Omega$, and $V_{DD}=5V$. 
Large Signal Amplifiers

DC biasing:
- Ensuring that the transistor has the correct dc level at its terminals.
- Termed as setting the Q-point, quiescent operating bias point.
- Same as setting the dc voltages and currents for the circuit with no signal applied.
Large Signal Amplifiers

The dc bias voltages and currents must be maintained even when the circuit is confronted with:

- Sources variations;
- Temperature changes;
- Change in component values due to manufacturing process inconsistencies.
Common Source Amplifier

\[
V_{GS} = V_{DD} \left[ \frac{R_2}{R_1 + R_2} \right]
\]

\[
V_{DD} = I_D R_D + V_{DS}
\]
Common Source Amplifier

\[ A_v = \frac{\Delta v_o}{\Delta v_i} \]
Self-Bias Circuit

- Useful for devices that require a negative gate-to-source voltage (depletion mode n-channel devices).
- Negative gate-to-source voltages are achieved by raising the source voltage higher than the gate voltage.
Self-Bias Circuit

\[ V_S = I_D R_S \]
\[ V_{GS} = -I_D R_S \]
\[ V_{DD} = I_D \left( R_D + R_S \right) + V_{DS} \]
Self-Bias Circuit

\[ +V_{DD} = 8 \text{ V} \]

\[ R_D = 1429 \ \Omega \]

\[ R_G = 1 \ \text{M} \Omega \]

\[ R_S = 571 \ \Omega \]

\[ C_1, C_2, C_S \]
Procedure

- Draw load line on the output curves of the transistor.
- Locate the Q-point on the load line.
- If there is a bypass capacitor in the circuit, then construct an ac load line with slope:
  \[ \text{slope} = \frac{1}{\text{total resistance within } S-D \text{ loop not shorted by } C} \]
- Calculate the large signal voltage gain.
Other FET Configurations

- Common source
- Common gate
- Common drain
BJTs

- Invented in 1947 in the Bell Laboratories.
- It revolutionized electronics, by replacing the vacuum tubes.
- Standard for the TTL (Transistor-Transistor-Logic) and ECL (Emitter-Coupled-Logic) families of logic devices.
BJT Structure

- Three-layer sandwich of alternating semiconductor materials.
- Two types:
  - NPN;
  - PNP.
- Terminals:
  - Emitter;
  - Base;
  - Collector.
BJT Structure

- Two $p-n$ junction diodes built very close together.
- The junction between base and emitter is called *emitter junction*, and the junction between base and collector is called *collector junction*. 
The emitter is placed on top of the collector with a very thin base between them, and the primary carrier flow is from the emitter to the collector.
Modes of Operation

- **Cutoff** – Both junctions are reverse biased and the transistor appears as an open switch.
- **Saturation** – Both junctions are forward biased and the transistor appears as a closed switch.
- These two bias conditions are important for digital circuits.
BJT Working as a Switch

Note the simplified interpretation of the BJT working as a switch in cutoff and saturation.

- Transistor in cutoff
- Both junctions reverse biased
- Open switch
- All terminal currents $\approx 0$

- Transistor in saturation
- Both junctions forward biased
- Closed switch
- Requires base current to maintain switch closed
BJT Models for Switching

$I_{B(SAT)}$ - the minimum base current to be exceeded for the transistor to be considered in saturation mode.
Modes of Operation

- **Active** – The emitter junction is forward biased and the collector junction is reverse biased.
- **Reverse active** – The emitter junction is reverse biased and the collector junction is forward biased.
Active Region

\[ I_E = I_B + I_C \]

Forward alpha
Forward common base current transfer ratio.

\[ \alpha_F = \left. \frac{I_C}{I_E} \right|_{\text{active region}} \]
Active Region

Forward common emitter current transfer ratio.

\[ I_C = \alpha_F I_E \]

\[ I_C = \alpha_F (I_B + I_C) \]

\[ I_C = \alpha_F I_B + \alpha_F I_C \]

\[ I_C - \alpha_F I_C = \alpha_F I_B \]

\[ I_C (1 - \alpha_F) = \alpha_F I_B \]

\[ \frac{I_C}{I_B} \bigg|_{\text{active region}} = \frac{\alpha_F}{(1 - \alpha_F)} = \beta_F \]
Ebers-Moll Model

Reverse alpha
Reverse common base current transfer ratio.

\[ \alpha_R = \frac{I_E}{I_C} \text{ reverse active bias} \]

\[ I'_E = I_{ES} \left( e^{\frac{qV_{BE}}{kT}} - 1 \right) \]

\[ I'_C = I_{CS} \left( e^{\frac{qV_{BC}}{kT}} - 1 \right) \]
Ebers-Moll Model

\[
I_E' = I_{ES} \left( \frac{q V_{BE}}{kT} - 1 \right)
\]

\[
I_C' = I_{CS} \left( \frac{q V_{BC}}{kT} - 1 \right)
\]

\[
I_E = I_{ES} \left( e^{\frac{q V_{BE}}{kT}} - 1 \right) - \alpha_R I_{CS} \left( e^{\frac{q V_{BC}}{kT}} - 1 \right)
\]

\[
I_C = I_{CS} \left( e^{\frac{q V_{BC}}{kT}} - 1 \right) - \alpha_F I_{ES} \left( e^{\frac{q V_{BE}}{kT}} - 1 \right)
\]
Common Emitter Amplifier

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{I_C}{\beta} \]

\[ V_{CC} = I_C R_C + V_{CE} \]
Common Source Amplifier

- Non-linear.
- Large variations in beta.
- Thermal runaway.
Self-Bias Circuit

- Useful to control the effects discussed in the previous slide.
- This circuit stabilizes collector current instead of base current, thus reducing the effects of beta variations and temperature on the quiescent operating point.
- Collector current is determined by the voltage across a resistor, $R_E$, placed in series with the emitter.
Self-Bias Circuit

\[ \frac{V_{CC}}{R_1 + R_2} \gg I_B = \frac{I_E}{\beta + 1} \]

\[ V_B = V_{CC} \frac{R_2}{R_1 + R_2} = V_{BE} + I_E R_E \]
Procedure

- Draw load line on the output curves of the transistor.
- Locate the Q-point on the load line.
- If there is a bypass capacitor in the circuit, then construct an ac load line with slope:

\[ \text{slope} = \frac{1}{\text{total resistance within S-D loop not shorted by } C} \]

- Calculate the large signal voltage gain.
Other BJT Configurations

Common emitter

Common base

Common collector