EE 2731  
Digital Logic Design Lab  
Fall 2007

Instructor: Gabriel A. de Souza  
Room 313 EE Building, Ph: 578-4831, email: gdesou1@lsu.edu

Office hours: 9:00-10:30 TWTh  
12:00-1:00 T

Lab Sections: 1 and 2

TA: To be announced  
Office hours: 
Lab Sections:

Prerequisites: EE2730

Text: Digital Logic Design Laboratory, Gabriel A. de Souza

Software Package: B²Logic.

Course Description: This course introduces the student to combinational and sequential circuit design and implementation. There will be ten experiments and each will comprise of a design, software simulation, and hardware implementation. Other issues pertaining to digital logic design will be addressed in the lectures.

Grading:  
Lab Experiments and Lab Quizzes: 50%  
Midterm (10/02 in class): 20%  
Final (12/04 in class): 20%  
Practical Finals (12/04 and 12/06 in the lab): 10%

At the discretion of the instructor a grading curve may be used to allow for a more favorable grade distribution.

Policy on Exams: Make-ups on Exams are allowed under extenuating circumstances, and they may be oral or written. All corrections to grading must be made within two weeks of exam return.