Department of Electrical & Computer Engineering
Louisiana State University

EE 3232 **Solid State Devices I** **Spring 2004**

Schedule: MWF: 12:40-1:30 PM (145 EE Building)
Catalog Description: Prereq: EE 2230 and EE 2130. Physics and analysis of basic semiconductor devices; principles of integrated circuit fabrication.

Text: Solid State Electronic Devices by B. G. Streetman and S. Banerjee, 5th ed., Prentice Hall 2000

References: 1) R. S. Muller and T. I. Kamins, "Device Electronics for Integrated Circuits," J. Wiley, 1977
2) S. Dimitrijev, "Understanding Semiconductor Devices," Oxford, 2000
3) R. F. Pirret, "Semiconductor Device Fundamentals," Addison Wesley, 1996.

Instructor: Dr. Pratul Ajmera, 221 EE Building, Ph: 578-5620, E-mail: ajmera@ece.lsu.edu

Office Hours: MWF: 9-10 AM and MW: 3:35-4:35 PM. Other times by appointment.

Goals: 1) Provide a sound understanding of operation of existing devices to enhance student's understanding in design, fabrication and operation of current devices and circuits and their future developments.
2) Develop tools that can be applied in design of new devices, their applications and in understanding of their operations.

Pre-requisite by Topics: Terminal properties of diodes and transistors, modern physics (sophomore level).

Topics: 1. Crystal properties and IC fabrication technology (5 classes)
2. Energy bands and charge carriers in semiconductors (8 classes)
3. Excess carriers in semiconductors (4 classes)
4. P-n junction (8 classes)
5. MOS structure (4 classes)
6. MOSFET (3 classes)
7. BJT (7 classes)
8. Tests and quizzes (3 classes)

The class times listed above are estimates and may be changed somewhat depending on student preparation and need.

Instructional Outcomes: At the end of the course, students should have
1. A clear understanding of the basic physics underlying the operation of current electron devices.
2. Rudimentary ability to relate device design and fabrication parameters to device performance.
3. Rudimentary understanding of factors that limit performances of current devices.

Estimated ABET Professional Component: Engineering Science: 100%

Course Outcome Assessment: 1) Class tests and quizzes, 2) Home assignments and 3) Final Exams.

Grading: Home assignments 10 %

Quizzes (Three)	15 %	(Mon – Feb. 9, Wed – Mar. 17 and Mon – Apr. 26). Each quiz is 5%.
Test 1	20 %	(Mon – Mar. 1)
Test 2	20 %	(Fri – Apr. 2)
Final Exams.	35 %	(Fri – May 14, 7:30-9:30 AM)
	100 %	

A letter grade is not attached to a particular numerical score per se. Relative standing in class along with the degree of difficulty of the tests will be factored in prior to arriving at the final letter grade for the course.

Issues regarding manufacturability and cost and yield economics are discussed pertaining to integrated circuits.