

EE 3755, Fall 2010

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Information about Test 2

The test 2 will take place on Wednesday November 10, 2010. The test will be closed books and closed notes. You will not be allowed to use calculators neither computers nor cell phones.

The materials for test 2 follow on the next pages.

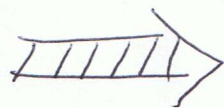
Materials for test 2

You are responsible for the following materials:

- 1) Verilog notes #1, #2, #3: You are responsible for everything from Verilog notes #1, #2, #3.
- 2) Verilog notes #4: You are responsible for everything except: (a) The event queue; (b) The testbench of notes #4.
- 3) Verilog notes #5: You are responsible for everything except the testbench of notes #5.

IMPORTANT NOTE ABOUT TEST BENCHES

I will not ask you to write Verilog code for testbenches. However, you are responsible for: (a) what is a testbench; (b) which are the tasks performed by a testbench.



NEXT PAGE.

Materials for test 2 cont.

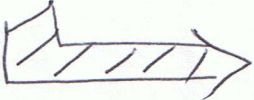
I gave you a one(1) page handout on testbenches addressing (a) and (b) of the previous page.

4) Verilog notes # 6: You are NOT responsible for anything from Verilog notes # 6.

5) Verilog # 7: You are responsible for everything.


6) Verilog # 8: You are responsible for everything except the testbench of notes # 8. CAREFULL: At the end of Verilog notes # 8 there is a module involving handshaking; (ready, start signals)
Pay attention to handshaking

7) Verilog notes # 9: You are ONLY responsible for the following:

 next page

Verilog notes # 9 cont: (a) The Verilog model for the sequential (clk) unsigned multiplier using the add/shift algorithm with handshaking; (ready, start signals); (b) The Verilog model for the sequential (clk) signed multiplier using the ~~the~~ Booth algorithm examining two (2) bits at a time with handshaking; (ready, start signals); (c) The Verilog model for the sequential (clk) signed multiplier using the Booth algorithm examining three (3) bits at a time with handshaking; (ready, start signals)

Important note 1: Pay attention to handshaking.


Important note 2: of course you need to know the algorithm for n-by-n unsigned multiplication using the add/shift algorithm,  next page

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Materials for test 2 cont.

(4)

Important note 2 cont: the Booth algorithm examining two (2) bits at a time and the Booth algorithm examining three bits at a time.

8) Verilog notes #10: You are only responsible for the IEEE 754 standard for floating point numbers Single Format.
No Verilog models for floating point hardware

9) Verilog notes #11: You are only responsible for: (a) what is synthesis; (b) The technology targets; (c) The facts that the initial block as well as delays cannot be ~~synthesized~~ synthesized; (d) The fact that the always block can sometimes be synthesized and sometimes not; (e) The names of the four steps of synthesis  next page.

Verilog notes # 11 cont. and ~~explanations~~
explanations about each of the four
steps of synthesis; (f) The fact that
~~the~~ the conditional operator is synthe-
sized as a multiplexer.

10) Verilog notes # 12 and # 12@ (figures):

You are responsible for everything
from Verilog notes # 12 and # 12@.

Number of points for test 2

The test 2 will have 107 points. 100
points on materials and 7 bonus points.

Bonus problem 1 (5 points): Write your
comments ahead of time. Don't put your
name on the comments.

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Number of points for test 2 cont:

Bonus problem 1 cont: Bring the comments during the day of test 2. Put them in the envelope provided to you and write your name outside of the envelope.

Bonus problem 2 (1 point): Was the test easy or difficult?

Bonus problem 3 (1 point): Was the given time enough?