Problem 1. write the register values after executing the following instructions.

	.text						
	.globl	__start					
	__start:						
0x400000	LOOP:	addi addi add	$a0 $a1 $s0	$zero $zero $a0	5 6 $a1	$a0=5 $a1=6 $s0=b	
		sll	$s0	$s0	2	$s0=2c	
		ori	$a0	$zero	0xffff	$a0=ffff	
		jal	LOOP			$ra=	$PC=400004
		nop				40001c	

Problem 2: Write a Machine code for the following instructions.

(Hexadecimal format)

add $7,$8,$9

addi $7,$8,5

0x01093820

0x21070005

Hint :

opcode for add is 0 and func field is 0x20.

opcode for addi is 8 .

Problem 3: Write MIPS program to print "*" character value of $t1 times.

(if $t1 value is 2, then print **: if $t1 value is 3, then print *, so on)..**
hint) data, text, global, system call,

Problem 4: Write MIPS program to count number of ones in register a0 and return the value in register $v0.

POP_CNT :

Jr $ra

Problem5: One way of making control signal is hardwired control.

5-1. What is the other way covered at the class?

5-2. What are the benefits of this over hardwired control?

Problem 6: compile the c code to the MIPS code.

```
for(i = 1;      i < b ;          i = i + d )  x = x ^ ( x<< 1);
```

register usage: b $s8 ; d $s9 ; i $s10 ; x $s11

sol).

Problem 7: Explain why loop unrolling makes the execution time shorter.

Problem 8: Performance of single cycle machine.

one program consists of 24% loads, 12%stores,
44% ALU instructions,18% branches
and 2% jumps(Instruction mix).

Assume operation times for the major functional units are following:
Memory units: 2 ns(nano seconds).
ALU and adders: 2 ns.
Register file(read and write): 1ns.

Instruction class	instruction memory	register read	ALU operation	Data memory	Register write	total
ALU type	2	1	2	0	1	6ns
Load	2	1	2	2	1	8ns
Store	2	1	2	2	0	7ns
Branch	2	1	2	0	0	5ns
Jump	2	0	0	0	0	2ns

1)What will the clock cycle for a single clock cycle machine?

##

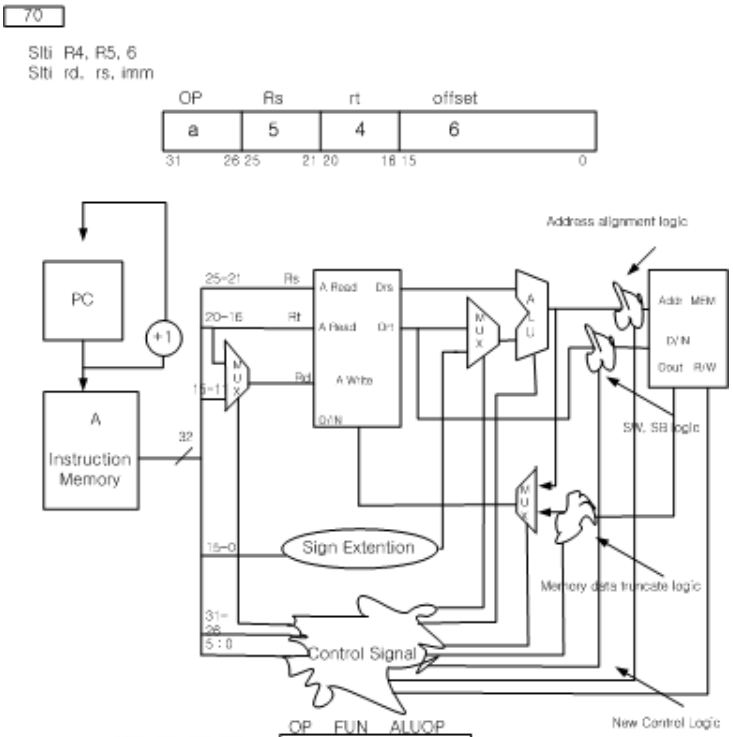
A machine with a variable clock will have a clock cycle that varies between 2ns and 8ns.

2)What will the average time per instruction for multi cycle machine ?

CPU clock cycle = 8*24% + 7 *12%+ 6*44%+ 5*18%+2*2%

= 6.6ns.

Problem 9: Modify the circuit to do the BNE instruction.



	OP	FUN	ALUOP
ADD R1, R2, R3	0	20	ADD
SUB R4, R5, R6	0	22	SUB
ADDi R7, R8, 5	8	X	ADD
OR R9, R10, R11	0	25	OR
LW R7, 8(R9)	23	X	ADD
LB R1, 2(R3)	20	X	ADD
SW R10, 11(R12)	2b	X	ADD
SB R10, 11(R12)	28	X	ADD
SLT R1, R2, R3	0	2a	SUB
SLTi R4, R5, 6	a	X	SUB

Problem 10: Compute this branch target address:

0x400000: BNE $r1,$r2,12….

Sol) 0x400034

Problem 11: Compute execution time and CPI.

The Finite State Diagram has 10 states.

state 0 takes 2 ns to finish.

Other states(state 1 to 9) take 2 ns to finish.

Instruction mix is following:

Memory access(LW and SW) is each 5%.

R-type is 70%.

BEQ is 10 %.

J is 10 %.

a)Compute single cycle CPI.

b)Compute multi cycle CPI.

c)Designers of new machine found out

new technology with 1 ns clock cycle and each state takes only(clock cycle should be multiple of 1ns)

0.9 ns except state 9 which takes 1.8 ns.

c-1) Compute single cycle CPI

c-2) Compute multi cycle CPI.

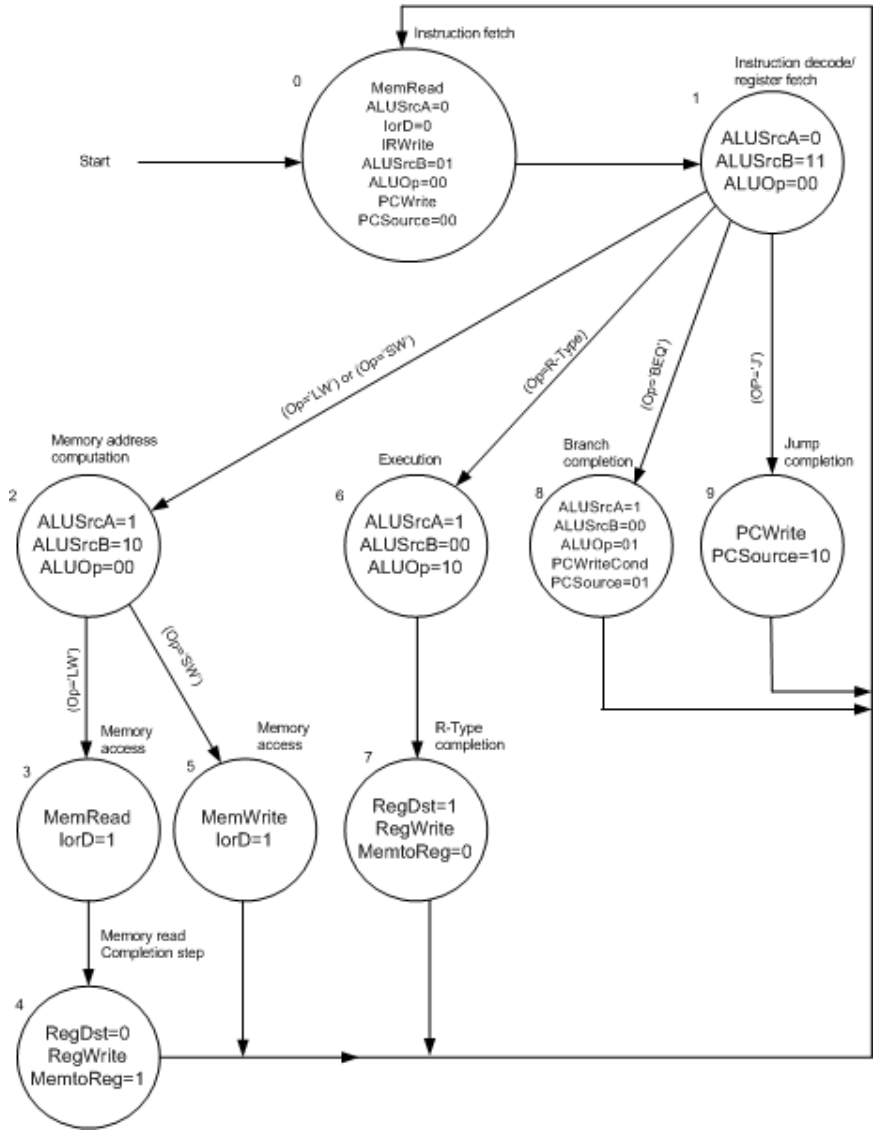
c-3) Designers found out a method to divide the state 9 into 2 states(the new 2 states, state 9-1 and state 9 -2) .

state 9-1 takes 1.1 ns.

state 9-2 takes 1.2 ns.

Is the performance better or worse?

(Why).



sol) a) longest path..so..5 * 2ns = 10 ns.

b) LW 5 * 2 * 0.05

SW 4 * 2 * 0.05

R-type 4 *2 * 0.7

BEQ 3 *2 * 0.1

J 3*2*0.1

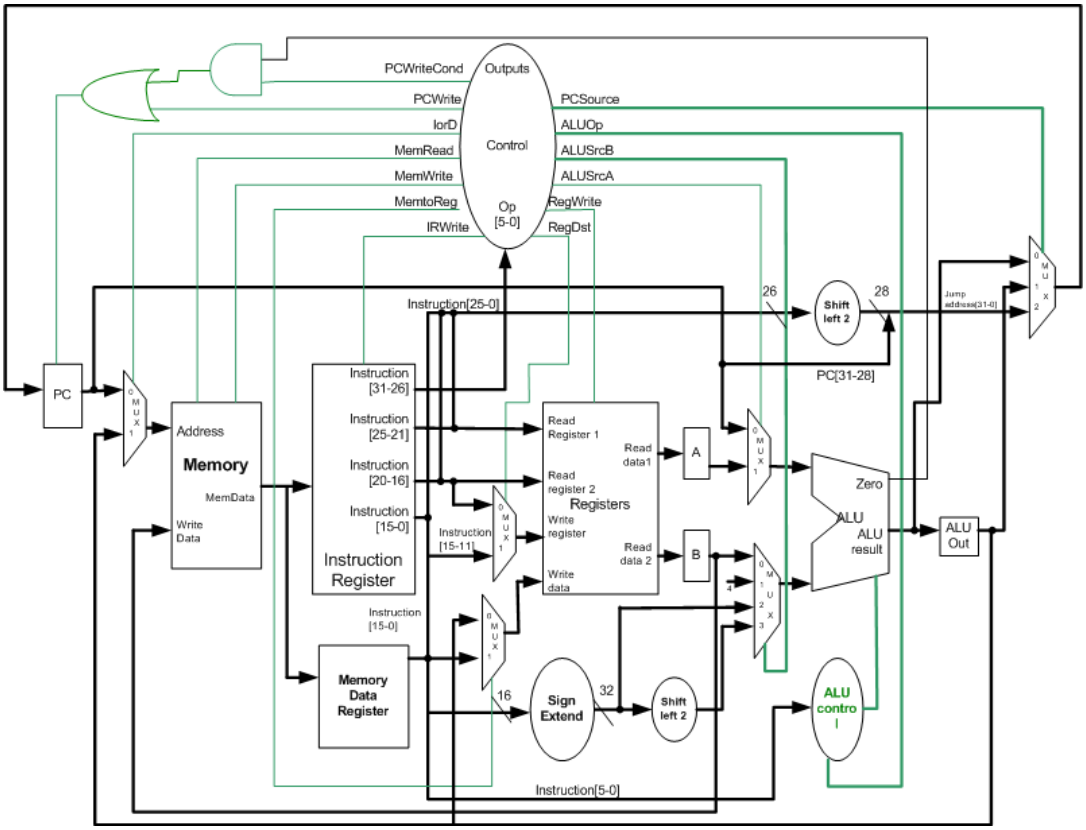
CPI = 5 * 2 * 0.05 + 4 * 2 * 0.05+ 4 *2 * 0.7

+ 3 *2 * 0.1+ 3*2*0.1;

c) worse because to finish 9-1,9-2 , we need 4ns.

Problem 12: Fill the table for SRC2 column.

Label	ALU control	SRC1	SRC2	Register control	Memory	PCWrite control	Sequencing
Fetch	Add	PC	#		Read PC	ALU	Seq
	Add	PC	#	Read			Dispatch 1
Mem1	Add	A	#				Dispatch 2
LW2					Read ALU		Seq
				Write MDR			Fetch
SW2					Write ALU		Fetch
Rformat 1	Func code	A	#				Seq
				Write ALU			Fetch
BEQ1	Subt	A	#			ALUOut-cond	Fetch
JUMP1						Jump address	Fetch


PCWriteCond
PCWrite
IorD
MemRead
MemWrite
MemtoReg
IRWrite
Outputs
Control
Op
[5-0]
PCSource
ALUOp
ALUSrcB
ALUSrcA
RegWrite
RegDst
Instruction[25-0]
26
Shift
left 2
28
PC[31-28]
Jump
address[31-0]
PC
M
U
X
Address
Memory
MemData
Write
Data
Instruction
[31-26]
Instruction
[25-21]
Instruction
[20-16]
Instruction
[15-0]
Instruction
Register
Instruction
[15-11]
Instruction
[15-0]
Memory
Data
Register
Read
Register 1
Read
register 2
Registers
Write
register
Write
data
Read
data1
Read
data 2
A
B
Zero
ALU
ALU
result
ALU
Out
16
Sign
Extend
32
Shift
left 2
ALU
contro
l
Instruction[5-0]