EE 3755: Computer Organization

Instructor:

Alexander Skavantzos
245 Electrical Engineering Building
Phone: 578-5240, Email: alex@ece.lsu.edu

Text:

"Computer Organization & Design," David A. Patterson & John Hennessy, 4th ed., 2008, Morgan Kaufmann

Reference:

"Verilog HDL," Samir Palnitkar

Catalog Description:

Computer Organization (3). Prereq: EE 2730
Structure and Organization of Computer systems; instruction sets.
Arithmetic; data path and control design.

Goals:

To familiarize students with computer organization and processor design.

Topics:

Basic of fixed and floating point computer arithmetic.
Introduction to Verilog.
Introduction to Digital Computers.
Instruction set architecture.
Hardwired and Micro program based control units.
MIPS

Grading:

Attendance	5%
Test 1:	23%
Test 2:	23%
Homework:	15%
Quizzes:	10%
Final Exam:	24%

Test Policy:

If a student misses any one of tests 1 or 2 for a medical reason then the student should provide the instructor with a doctor's statement stating that the student was sick on the day of the test. In this case, a make-up test will <u>NOT</u> be given but instead the remaining test will count for 32.5%, the homework, for 20%, the quizzes 10%, the attendance 5% and the final for 32.5%
Homework Policy: Late homework will <u>not</u> be accepted.