

EE 3755

Computer Arithmetic

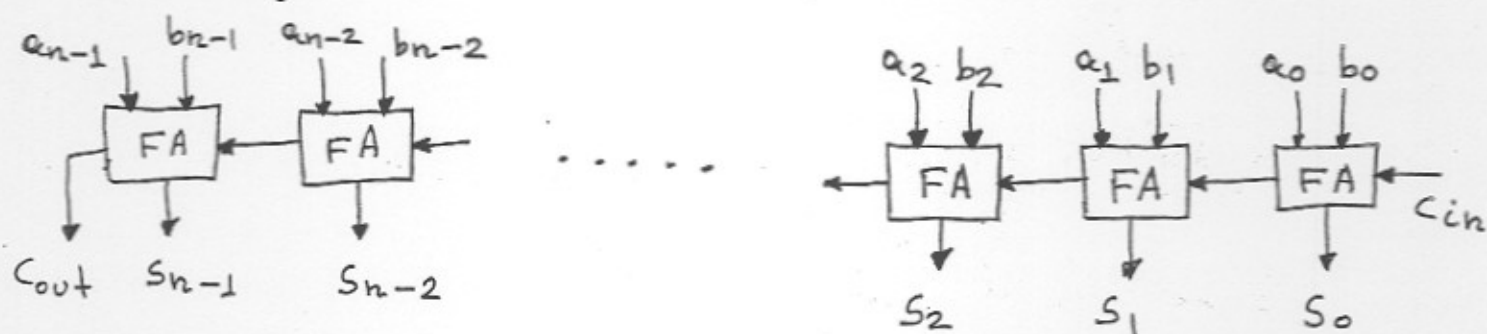
Handout # 10

## Ripple Carry Adder

Consider two  $n$ -bit binary numbers

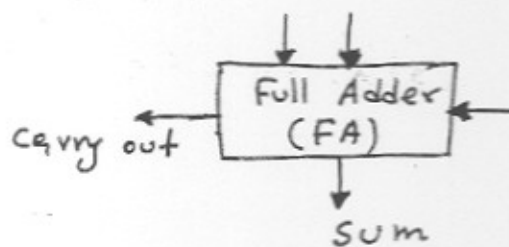
$$A = (a_{n-1} a_{n-2} \dots a_1 a_0)_2 ; B = (b_{n-1} b_{n-2} \dots b_1 b_0)_2$$

One two-operand adder (adding  $A$  and  $B$ ) is the ripple carry adder shown below:



where

FA indicates Full Adder



The delay through an  $n$ -bit ripple carry adder is  $n \times D_{FA}$  where  $D_{FA}$  is the delay through a Full Adder

## Unsigned array multipliers

Consider two 5-bit unsigned numbers  $A = a_4 a_3 a_2 a_1 a_0$  and  $B = b_4 b_3 b_2 b_1 b_0$  where  $a_4$  and  $b_4$  are the most significant bits of  $A$  and  $B$  while  $a_0$  and  $b_0$  are the least significant bits of  $A$  and  $B$  respectively.

The table below describes the multiplication operation.

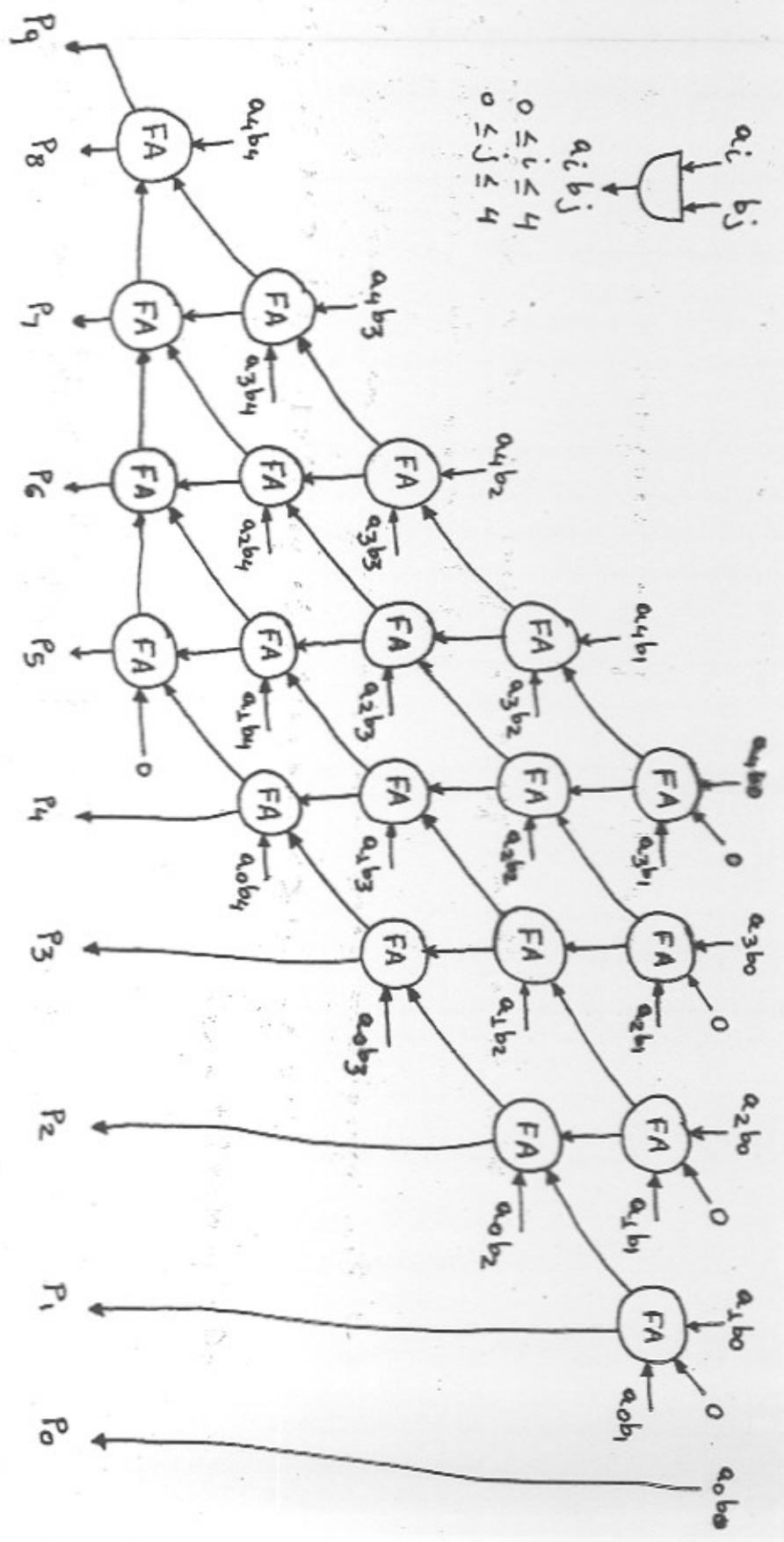
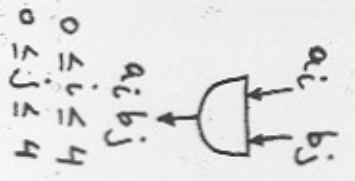
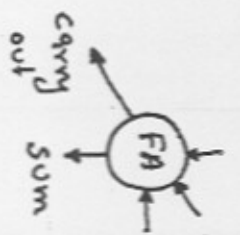
$$\begin{array}{r}
 a_4 a_3 a_2 a_1 a_0 = A \\
 \times) \quad b_4 b_3 b_2 b_1 b_0 = B \\
 \hline
 a_4 b_0 a_3 b_0 a_2 b_0 a_1 b_0 a_0 b_0 \\
 a_4 b_1 a_3 b_1 a_2 b_1 a_1 b_1 a_0 b_1 \\
 a_4 b_2 a_3 b_2 a_2 b_2 a_1 b_2 a_0 b_2 \\
 a_4 b_3 a_3 b_3 a_2 b_3 a_1 b_3 a_0 b_3 \\
 +) \quad a_4 b_4 a_3 b_4 a_2 b_4 a_1 b_4 a_0 b_4 \\
 \hline
 P_9 \quad P_8 \quad P_7 \quad P_6 \quad P_5 \quad P_4 \quad P_3 \quad P_2 \quad P_1 \quad P_0 = P
 \end{array}$$

Summand matrix describing the add-shift operations in a 5-by-5 unsigned multiplication

- In the above, every term  $a_i b_j$  denotes the AND operation between bits  $a_i$  and  $b_j$ . Each term  $a_i b_j$  is called a summand.
- $P_9$  and  $P_0$  are the most significant and least significant bits of the product respectively.

(2)

Note



A 5-by-5 unsigned array multiplier.

- The cost of an  $n$ -by- $n$  unsigned array multiplier will be  $n^2$  AND gates plus  $n \times (n-1)$  FAs
- The delay through an  $n$ -by- $n$  unsigned array multiplier will be Delay of AND +  $(n-1) \times$  Delay of FA +  $(n-1) \times$  Delay of FA =  $D_{AND} + 2 \times (n-1) \times D_{FA}$ .

