EE 3755, Spring 2003

Solutions of HW #4

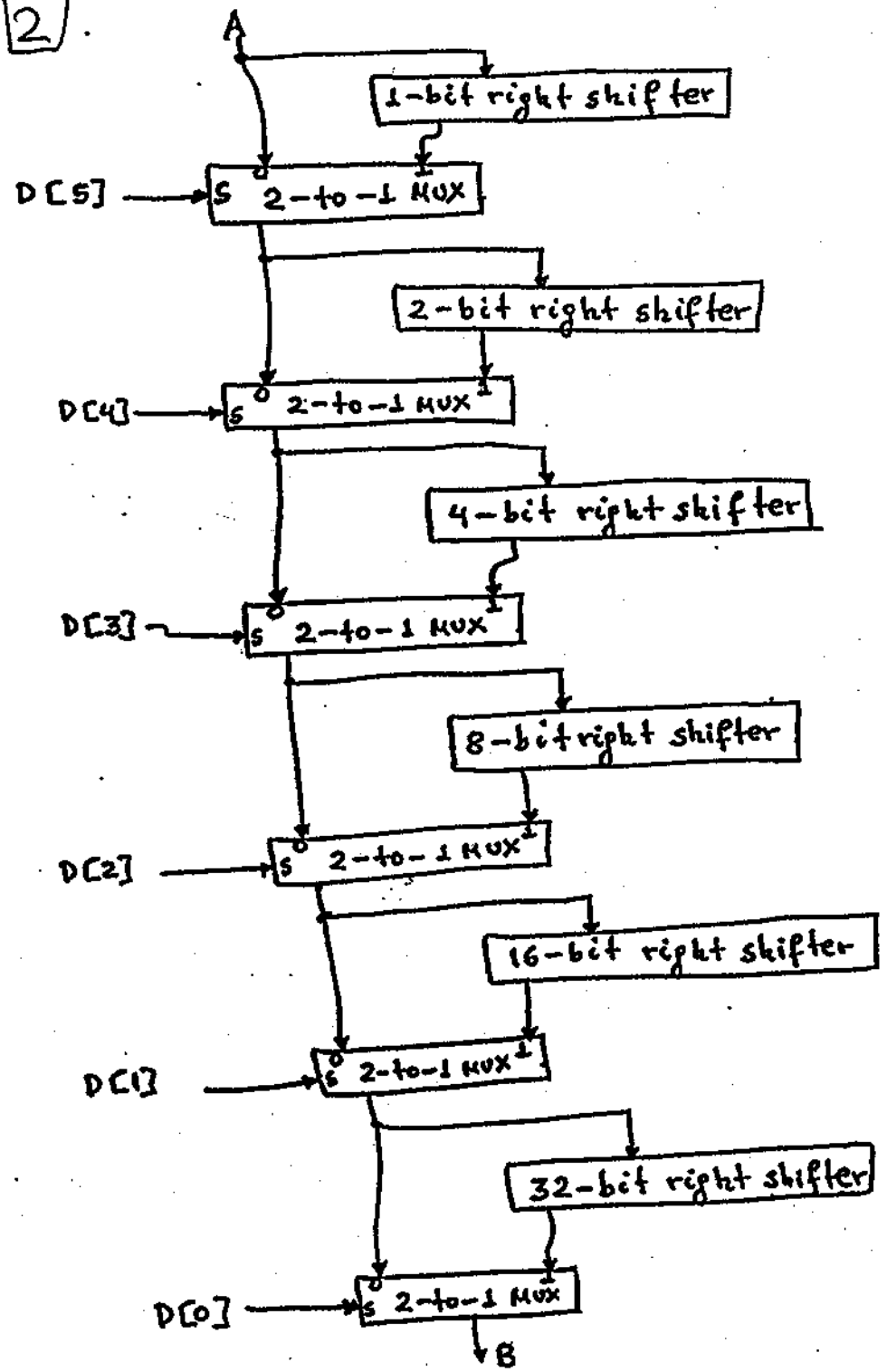
EE 3755, [redacted] (1)

Solutions of Homework #4

1 (a) Regarding a 32-bit arithmetic instruction with indirect addressing mode, the controller visits the steps 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 16, 19, 22. Therefore, the time required for completely handling the above instruction is $15 \times 10\,ns = 150\,ns$; (recall that each visit over each step is of duration 10ns = clock period)

(b) Regarding a couple of two-address 16-bit instructions located next to each other in the same memory word, the controller visits steps 1, 2, 3, 4, 50, 51, 52, 53, 100, 101, 50, 51, 52, 53, 100. Therefore, the time required for completely handling the above mentioned couple of instructions is $15 \times 10\,ns = 150\,nseconds$.

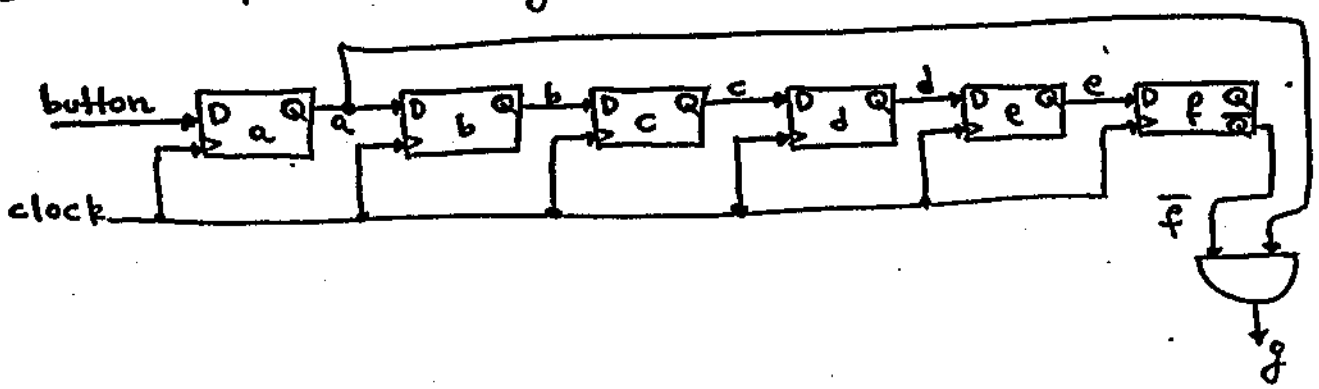
2.



** D = D[0], D[1], D[2], D[3], D[4], D[5] = shift amount.

most signif. bit ↑ ↑ least signif. bit.

(3) One possible design is the one shown below:



The design shown by the figure above consists of six flip-flops named a, b, c, d, e, f. The input signal named "button" is the signal coming from the asynchronous push button and has a long duration (40 clock periods for example). The output of the circuit is the signal "g" which is synchronous to the clock and has a duration of 5 clock periods. The flip-flop "a" acts as a synchronizer while flip-flops b, c, d, e, f delay the signal "a" by 5 clock periods.

** If you wish, you can construct a timing diagram of the signals button, a, b, c, d, e, f, $\overline{f}$ and g so that you understand how the above design operates.

4

(a)

$$
\begin{array}{r}
a_5\ a_4\ a_3\ a_2\ a_1\ a_0 = A \\
b_3\ b_2\ b_1\ b_0 = B \\
\hline
a_5b_0\ a_4b_0\ a_3b_0\ a_2b_0\ a_1b_0\ a_0b_0 \\
a_5b_1\ a_4b_1\ a_3b_1\ a_2b_1\ a_1b_1\ a_0b_1 \\
a_5b_2\ a_4b_2\ a_3b_2\ a_2b_2\ a_1b_2\ a_0b_2 \\
a_5b_3\ a_4b_3\ a_3b_3\ a_2b_3\ a_1b_3\ a_0b_3 \\
\hline
\text{Product} = P = p_9\ p_8\ p_7\ p_6\ p_5\ p_4\ p_3\ p_2\ p_1\ p_0
\end{array}
$$

The summands are the terms $a_i b_j$. P_9 is the most significand bit of the product while P_0 is the least significant bit

(5)

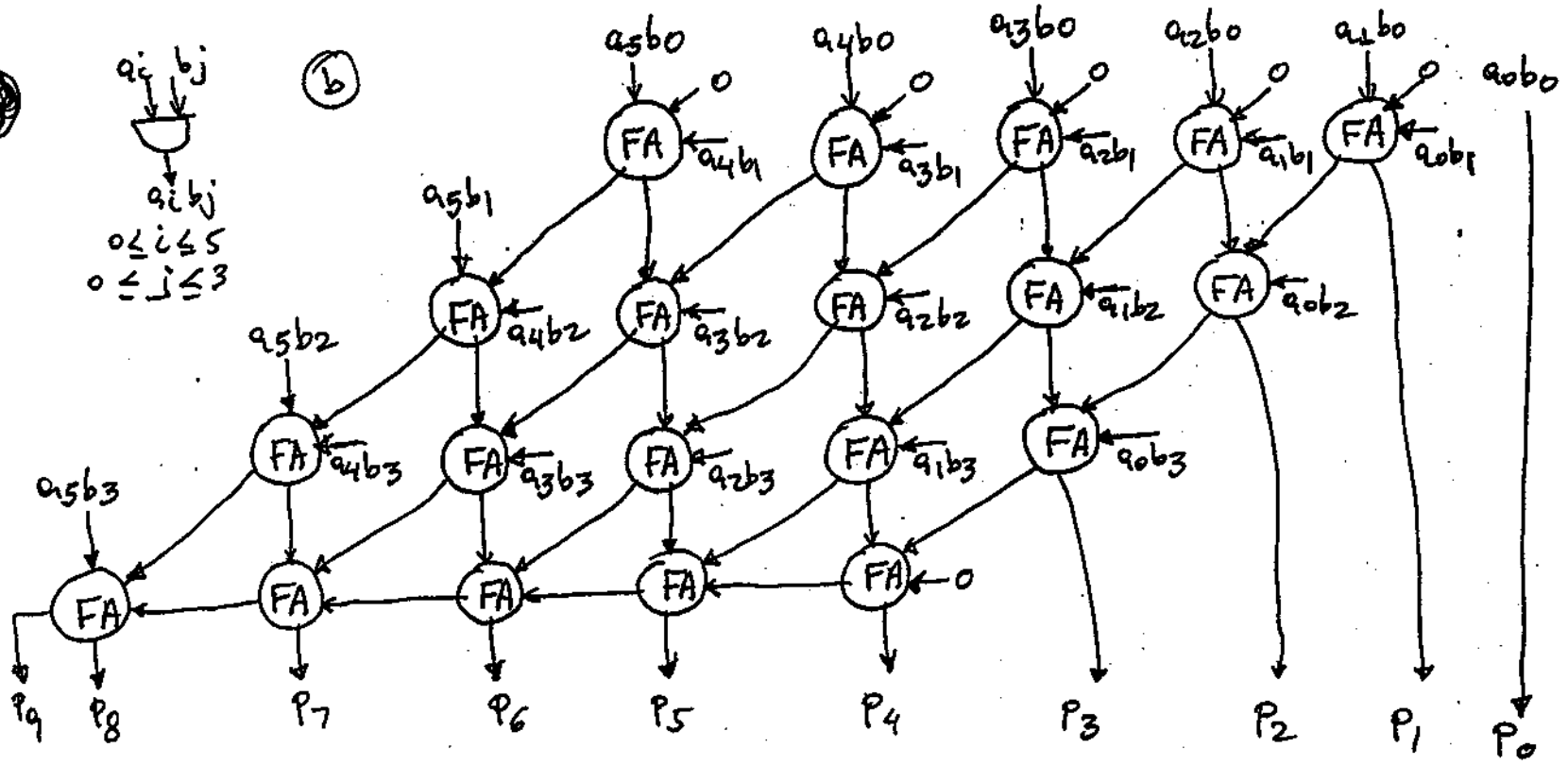
$a_i\ b_j$

$a_i b_j$

$0 \le i \le 5$

$0 \le j \le 3$

(b)



(c) $\text{Delay} = D_{AND} + (3+5)D_{FA} = D_{AND} + 8D_{FA}$.