

**Spring 2006**  
**EE 3755: Computer Organization**

**Instructor:**

Alexander Skavantzios  
245 Electrical Engineering Building  
Phone:578-5240  
E-mail:alex@ece.lsu.edu

**Text:**

“Computer Organization & Design,” David A. Patterson & John Hennessy.

**Reference:**

“Verilog HDL,” Samir Palnitkar,

**Catalog Description:**

Computer Organization(3). Prereq: EE 2730.  
Structure and Organization of computer systems; instruction sets;  
Arithmetic; data path and control design.

**Goals:**

To familiarize students with computer organization and processor design.

**Topics:**

Basic of fixed and floating point computer arithmetic.  
Introduction to Verilog.  
Introduction to Digital Computers.  
Instruction set architecture.  
Hardwired and Micro program based control units.  
MIPS.

**Grading:**

Test 1 : 25%  
Test 2 : 25%  
Homework : 15%  
Quizzes : 10%  
Final Exam : 25%

**Test Policy :**

If a student misses any one of tests 1 or 2 for a medical reason, then the student should provide the instructor with a doctor's statement stating that the student was sick on the day of the test. In this case, a make-up test will NOT be given but instead the remaining test will count for 35%, the homework for 20% , quizzes for 10% and the final for 35%.

**Homework Policy :**

Late homework will not be accepted.

