

Spring 2005
EE 3755: Computer Organization

Instructor:

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Text:

"Computer Organization & Design," David A. Patterson & John Hennessy.

Reference:

"Verilog HDL," Samir Palnitkar,

Catalog Description:

Computer Organization (3). Prereq: EE 2730.
Structure and Organization of computer systems; instruction sets;
Arithmetic; data path and control design.

Goals:

To familiarize students with computer organization and processor design.

Topics:

Basic of fixed and floating point computer arithmetic.
Introduction to Verilog.
Introduction to Digital Computers.
Instruction set architecture.
Hardwired and Micro program based control units.
MIPS.

Grading:

Test 1 : 25%
Test 2 : 25%
Homeworks : 15%
Final Exam : 35 %

Test Policy : If a student misses any one of tests 1 or 2 for a medical reason, then the student should provide the instructor with a doctor's statement stating that the student was sick on the day of the test. In this case, a make-up test will NOT be given but instead the remaining test will count for 35%, the homeworks for 20% and the final for 45%.

Homework Policy : Late homework will not be accepted.