

Spring 2012

EE 2720: Digital Logic I

General:

Units 2 hrs. Spring Semester (2011-12), 7:40 am – 8:30 am MW (1109 Patrick Taylor Hall Building)

Catalog Data:

Digital Logic I (2). Prereq: MATH 1550. Boolean algebra; logic gates; minimization methods; analysis and synthesis of combinational logic networks; design examples.

Textbook:

“Fundamentals of Digital Logic with Verilog Design”, Second edition, Stephen Brown and Zvonko Vranesic, McGraw-Hill, 2008.

Goals:

This course provides a basic knowledge of binary number systems, Boolean algebra, logic gates and minimization methods.

Prerequisite:

Math 1550.

Topics:

1. Analog versus digital, binary octal, hexadecimal numbers, binary arithmetic, codes (3 classes).
2. Boolean algebra (3 classes).
3. Logic gates (2 classes).
4. Representation of logic functions; canonical sum; canonical product (2 classes).
5. Minimization methods (4 classes).
6. Analysis of combinational logic circuits (1 class).
7. Design of combinational logic circuits (6 classes).
8. Programmable logic devices (1 class).
9. Hardware Description Languages (3 classes)
10. Tests (2 classes).

Instructional Outcomes:

At the end of the course, the students should be able to:

- Understand the difference between analog and digital systems.
- Understand binary and hexadecimal number systems.
- Understand Boolean algebra.
- Design combinational logic circuits.
- Simplify Boolean functions and combinational logic circuits.
- Understand the function of decoders, encoders, priority encoders, multiplexers, adders and design with these components.
- Describe a combinational logic circuit using hardware Description Language.

Computer Usage:

None.

Design Experience:

This course provides design experience in designing combinational logic circuits.

Estimated ABET Professional Component:

Engineering Science: 1 credit.

Engineering Design: 1 credit.

Grading:

5-6 Homeworks	20%
2 Tests	50%
Final	30%

Test & Homework Policy:

If a student misses any one of tests 1 or 2 for a medical reason then the student should provide the instructor with a doctor's statement stating that the student was sick on the day of the test. In this case, a make-up test will NOT be given but instead the remaining test will count for 35%, the homework, for 20%, and the final for 45%. Late homework will not be accepted.

Instructor:

Alexander Skavantzios, Associate Professor; ECE department; office hours (9:00 – 11:00 AM Monday and Wednesday, 10:00 to 11:00 AM Friday) or by appointment; 245 EE Building

Relation of Course to Student Outcomes
(ABET requirement)
EE 2720 – Digital Logic I

The course contributes to these outcomes	Explanation
1. An ability to apply knowledge of mathematics, science, and engineering.	Many problems worked in this course require the use of mathematics and engineering.
3. An ability to design a system, component, or process to meet desired needs.	The course will teach the students how to implement in hardware combinational logic circuits as well as how to implement large combinational logic circuits using smaller ones.
5. An ability to identify, formulate and solve engineering problems.	Some of the problems assigned to the students are stated at a level that requires the students to identify, formulate and solve engineering problems.
11. An ability to use techniques, skills, and modern engineering tools necessary for engineering practice.	The course introduces the students to modern hardware design concepts and tools, such as hardware description languages.

Prepared by: Alexander Skavantzoz **Date:** Spring 2012