

EE 2720, Spring 2012

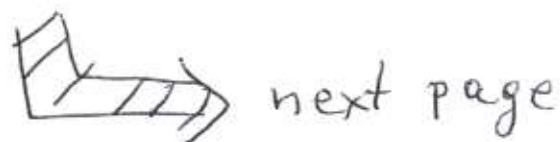
Information about the Final Exam

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A) The EE 2720 Final Exam will take place on Saturday May 12, 2012 from 5:30pm to 7:30pm. The exam will be closed books and closed notes. You will not be allowed to use calculators neither computers nor cell phones.

• IMPORTANT NOTE : DO NOT miss the final exam.

The materials for which you will be responsible for the final exam follow on the next pages



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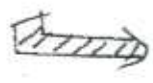

About the Final Exam cont.

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B) Materials for the Final Exam.

You will be responsible for the following materials.

- 1) Handouts # 0, #1, #2, #3, #4: You are not responsible for handouts # 0 to #4.
- 2) Handout #5: You are responsible for everything in handout #5. That is to say that you should know all the theorems presented in handout #5 as well as you should be able to prove them. Of course you should also know the axioms presented in handout #5.
- 3) Handouts #6 and #7: You are not responsible for handouts #6 and #7.
- 4) Handout #8: You are responsible for everything in handout #8.

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Materials for the final exam cont.

- 5) Handout # 9: You are responsible for everything in handout # 9.
- 6) Handout # 10: You are not responsible for handout # 10
- 7) Handout # 11: Here start reading from wherever it says "The 2-input Exclusive OR (XOR) gate and the 2-input Exclusive NOR (XNOR) gate" and read until the end of handout # 11
- 8) Handouts # 12 and # 13: You are not responsible for handouts # 12 and # 13.
- 9) Handout # 14: Here start reading from wherever it says "Karnaugh maps" and read until the end of handout # 14
- 10) Handouts # 15, # 16, # 16a, # 17, # 18, # 19, # 20, # 21: You are responsible for everything in handouts # 15, # 16, # 16a, # 17, # 18, # 19, # 20, # 21.

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About the final exam cont.

Materials for the final exam cont.

From EE 3755 materials you are responsible for the following:

a) Verilog notes # 1: Here start reading from the ~~beginning~~ point where it says "Module" and read until the end of Verilog notes # 1

b) Verilog notes # 2: You are responsible for the entire Verilog notes # 2.

← END OF MATERIALS →