EE 2720

Handout # 22.

- Ripple Carry Adders

Consider two n-bit numbers

$A = a_{n-1} a_{n-2} \ldots a_1 a_0$

$B = b_{n-1} b_{n-2} \ldots b_1 b_0$

One circuit that can add them is the <u>ripple carry adder</u>. An n-bit ripple carry adder is shown in figure 1:
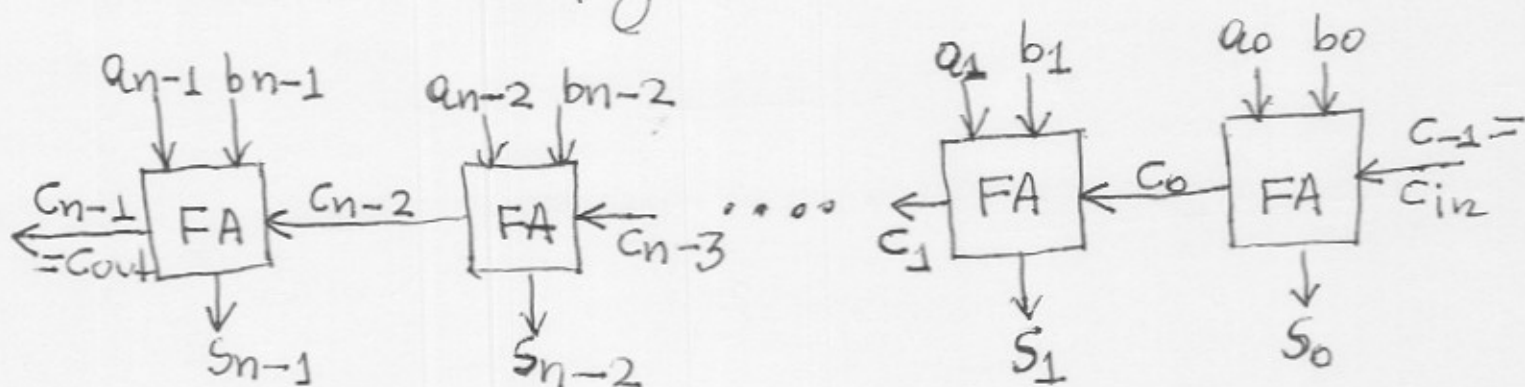

Fig. 1: An n-bit ripple carry adder.

In the above fig. 1, FA means full adder. By now you know what a full adder is and how to design it; (look at HW#6). Also, in the above fig. 1, $S_0, S_1, \ldots, S_{n-2}, S_{n-1}$ are the sum bits, while $C_0, C_1, \ldots, C_{n-2}, C_{n-1}$ are the carry-out bits; $C_{-1} = C_{in}$ is the overal carry-in to the n-bit ripple carry adder, while C_{out} is the overal carry-out

You can use the n-bit ripple carry adder

of fig. 1 to perform the addition $A+B$
or the subtraction $A-B = A + two's-complement of B$
$= A + one's$ complement of $B + 1$. If you want to
perform $A+B$, then you set the cin to
$cin = 0$; if you want to perform $A-B$, then
you must use $b'_{n-1}, b'_{n-2}, \ldots, b'_1, b'_0$ instead
of $b_{n-1}, b_{n-2}, \ldots, b_1, b_0$ and $c_{in} = 1$.

• Propagation Delay: The propagation delay
(worst case delay) through the n-bit ripple
carry adder of fig. 1 is $D_{ripple} = n \times D_{FA}$, whe-
re $D_{FA} = $ worst case propagation delay
through a full adder. As a comment, what
I have to say here is that the ripple carry
adder, although it is a very simple design,
it is also very slow. Its propagation delay is
directly proportional to the length of the
numbers that are added; you double the len-
gth, the delay gets double etc...

• A faster, but more expensive adder design,
is the Carry Lookahead Adder not to be pre-
sented here in EE 2720. You will learn
about it in EE 3755 if you take it; I teach
this course.

• Cascading (connecting) ripple carry adders:

Example 1: Using two 4-bit ripple carry

adders, design an 8-bit ripple carry ③
adder.
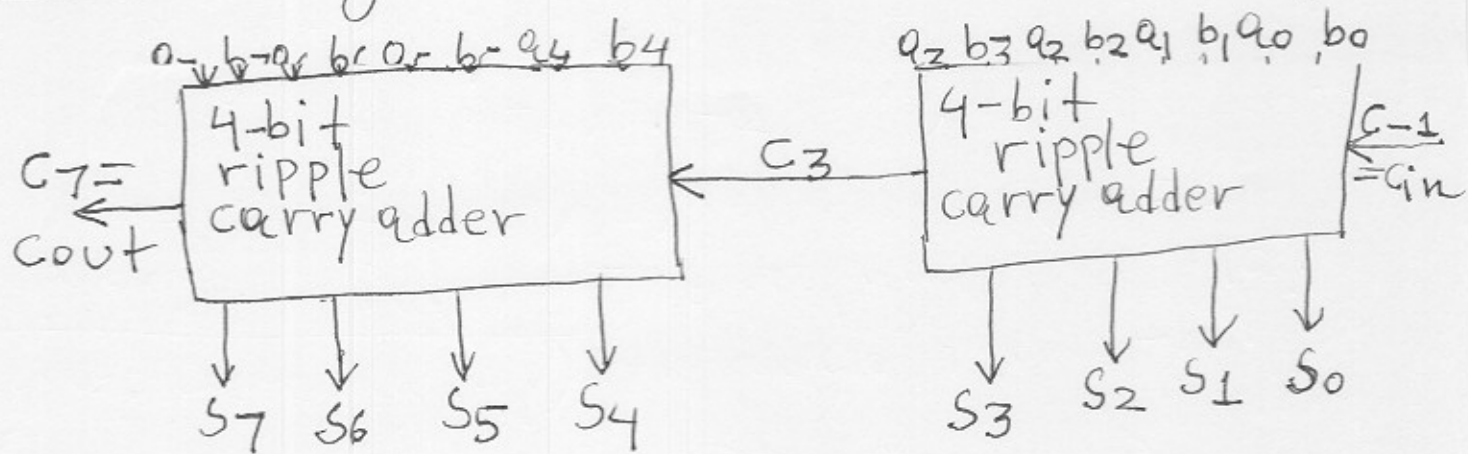
Answer: Figure 2 below shows the design:

Fig. 2: An 8-bit ripple carry adder constructed from two 4-bit ripple carry adders. Here, the two numbers to be added are $A = a_7 a_6 \cdots a_1 a_0$ and $B = b_7 b_6 \cdots b_1 b_0$.

Note: The above topic on ripple carry adders is optional in your textbook, but I thought it would be a good idea presenting it. Anyways, I also do this in EE 3755.